Bit Streams

Networks and Embedded Software

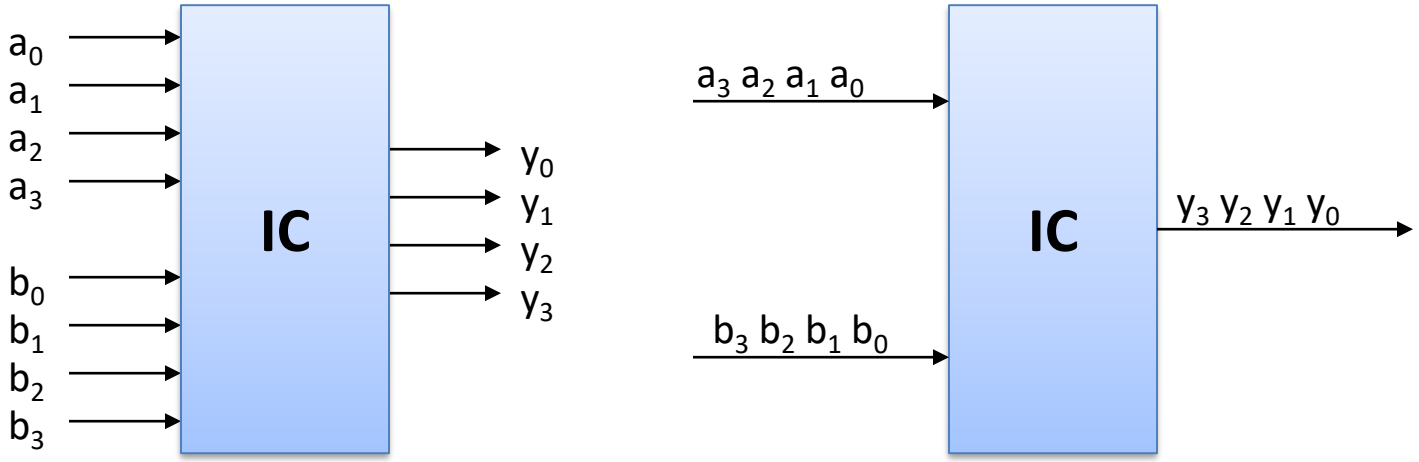
Module 3.3.3 (optional)

by Wolfgang Neff

cc BY NC ND

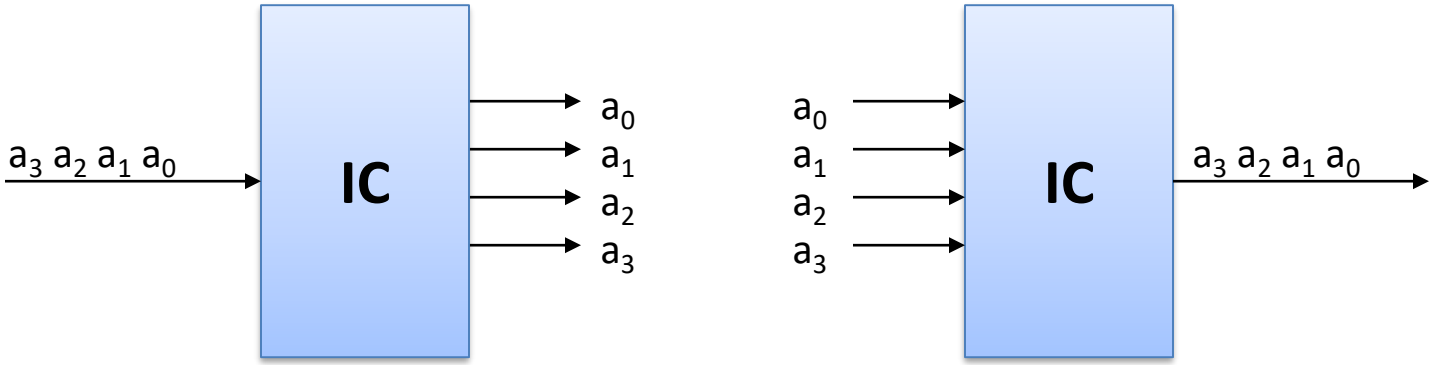
Serial / Parallel (1)

- Bits can come parallel or serially
  - Parallel: all at a time
  - Serial: one after another



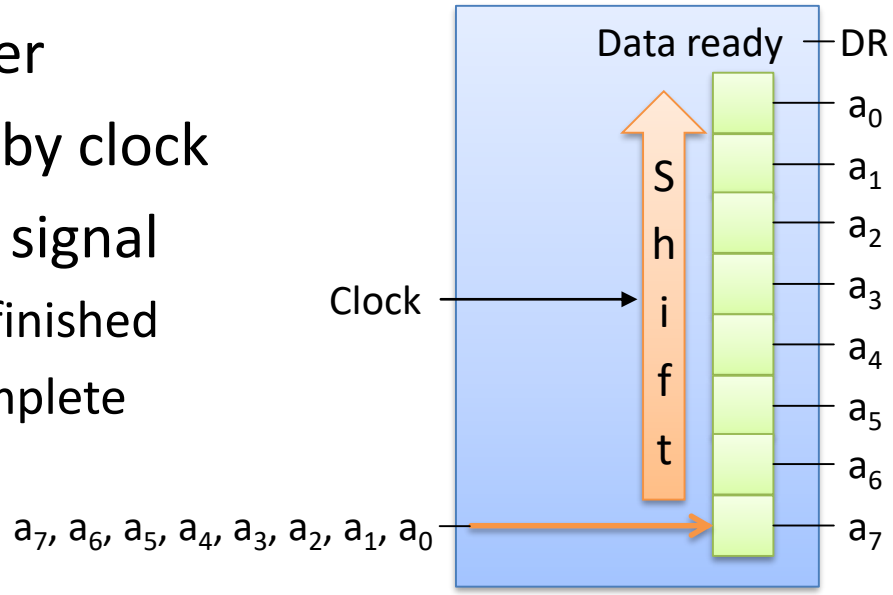
Serial / Parallel (2)

- Serial-to-parallel converter
  - Converts serial signals to parallel signals
    - A parallel-to-serial converter does it in reverse



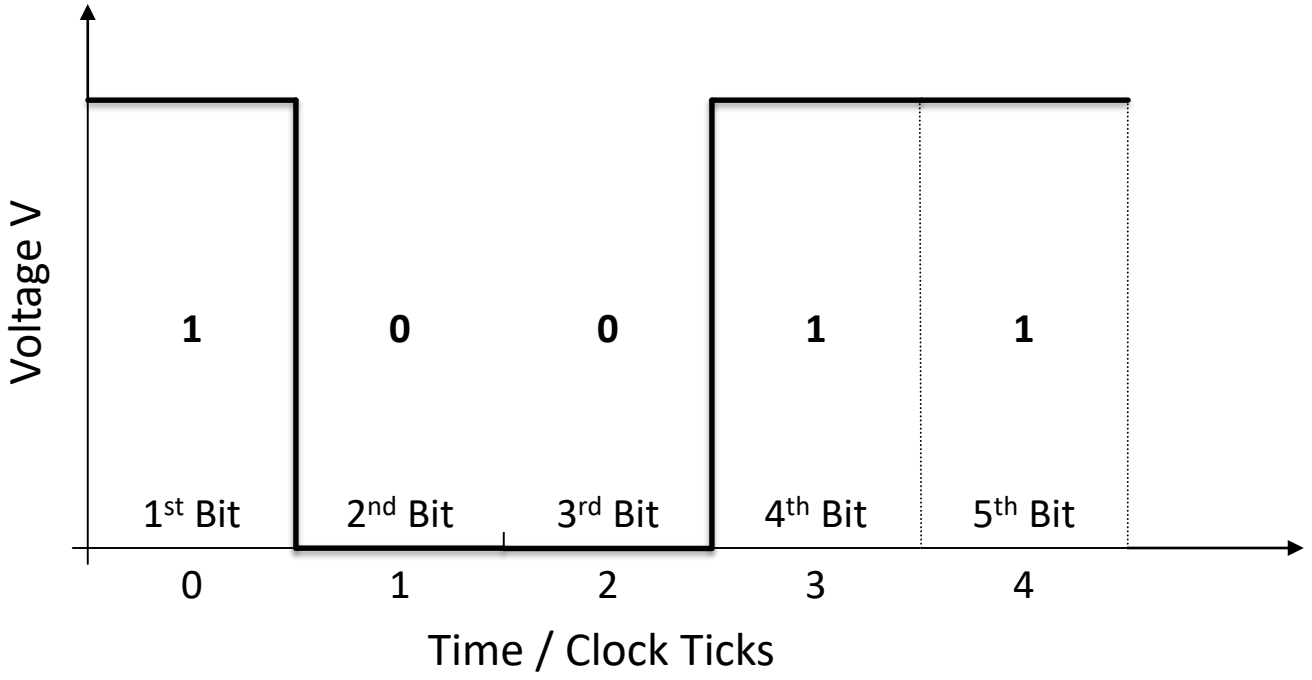
Serial / Parallel (3)

- Serial-to-parallel converter
  - Implementation
    - Shift register
    - Controlled by clock
    - Data ready signal
      - Shifting finished
      - Data complete



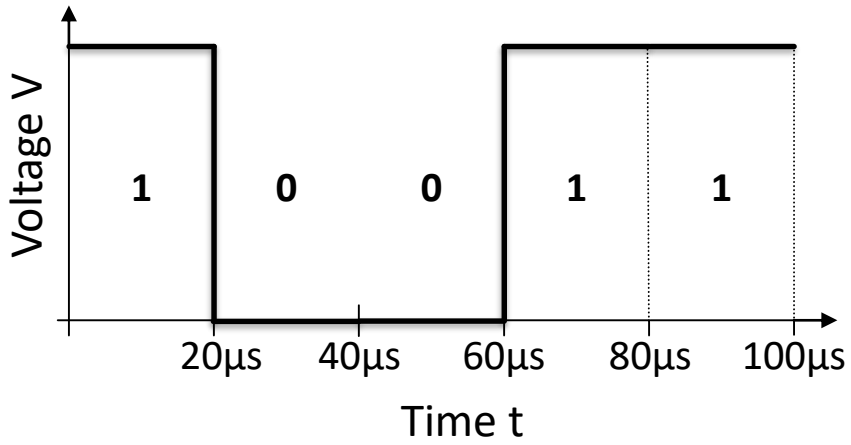
Serial / Parallel (4)

- Serial bits are a sequence of pulses
  - Example: 10011



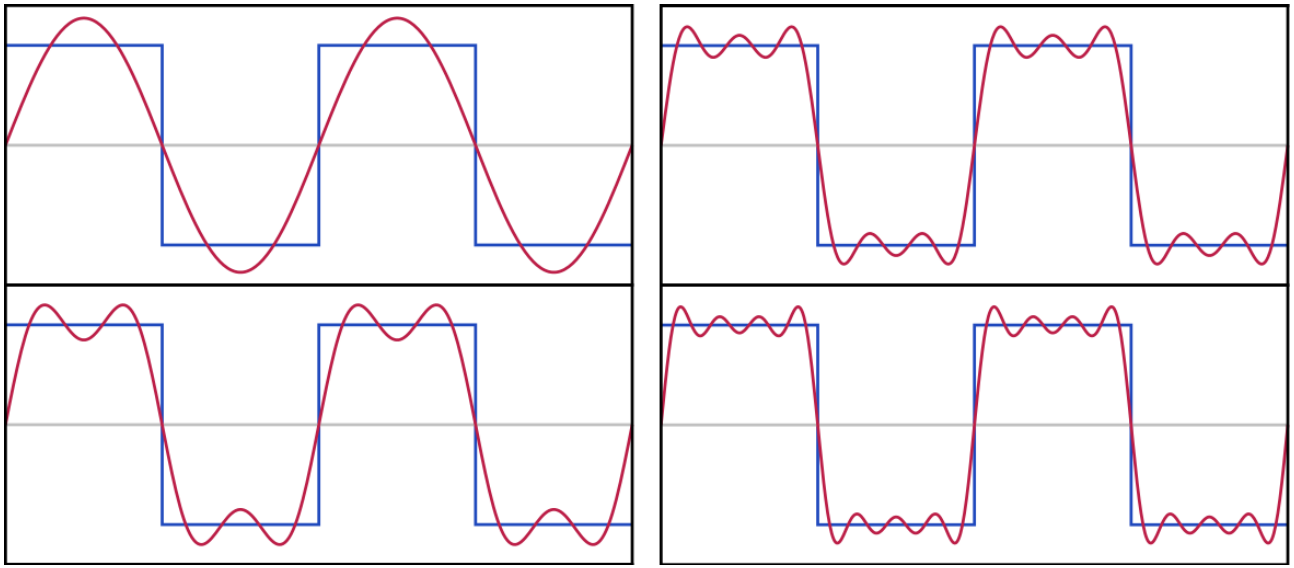
Serial / Parallel (5)

- Characteristics
  - Period T: duration of one pulse
  - Frequency f: number of pulses per second
  - Example
    - 50 kbps
      - Bits per second
    - f = 50 kHz
    - T = 20 µs



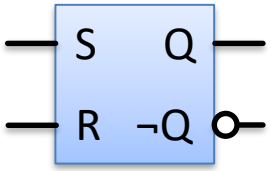
Serial / Parallel (6)

- Square pulses are an ideal conception
  - High frequencies are cut off
  - Square pulses become fuzzy



SR Latch (1)

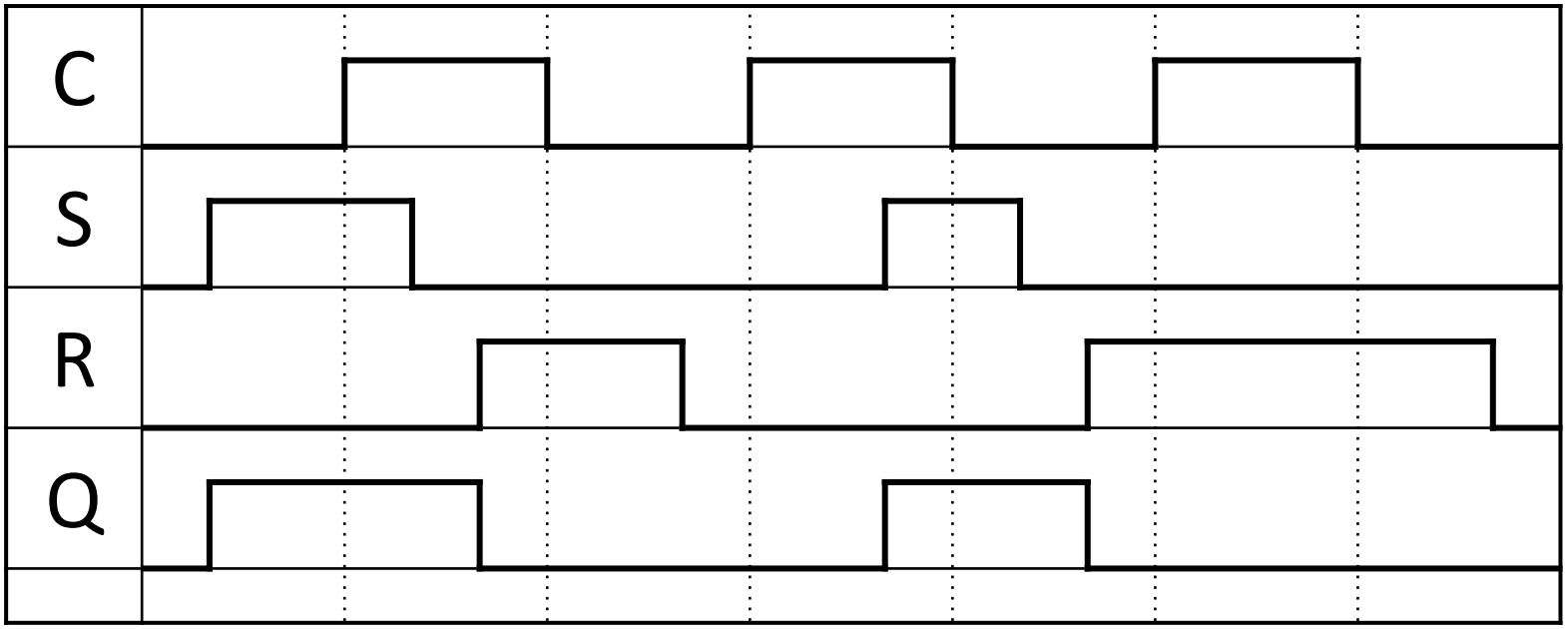
- Used to store information
  - Stores one bit
  - Control lines
    - *S*: Set bit
    - R: Reset bit
  - Stored information
    - Q: State



S	R	Q^+	Action
0	0	Q	Store
0	1	0	Reset
1	0	1	Set
1	1	X	Invalid

SR Latch (2)

- Time diagram of an asynchronous SR latch
  - Clock signal is of no importance

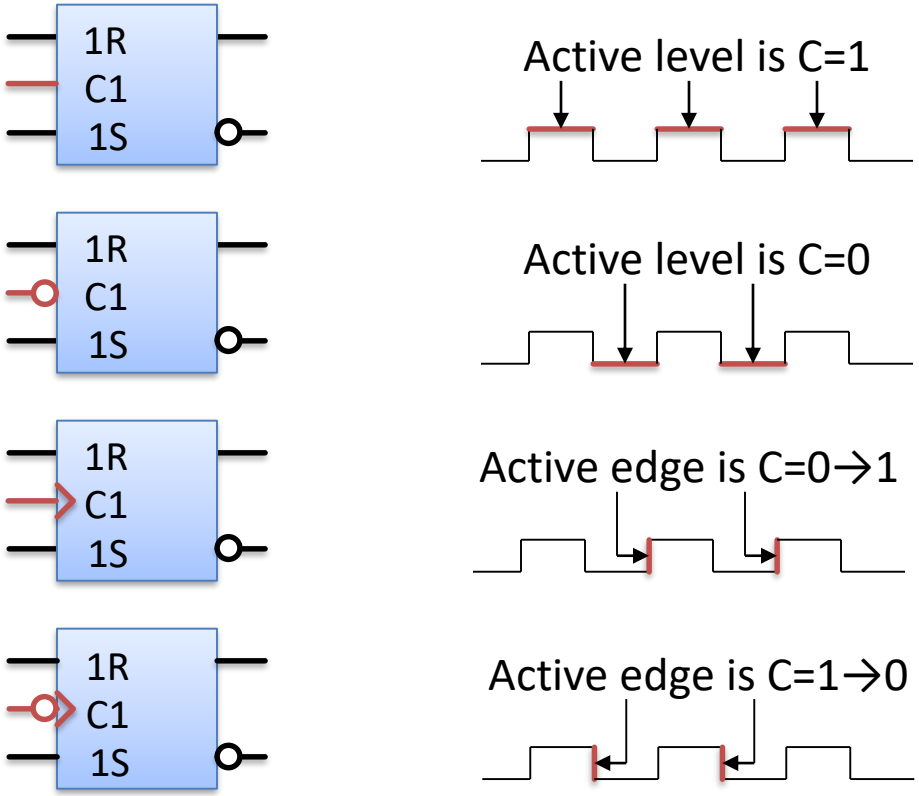


Triggers (1)

- Control when data are read
  - Active state: input data is read
  - Passive state: input data is ignored
  - Level triggers
    - Active state depends on the level
    - Level 0 or 1 is active
  - Edge triggers
    - Active state depends on the level change
    - Edge 0→1 or edge 1→0 is active

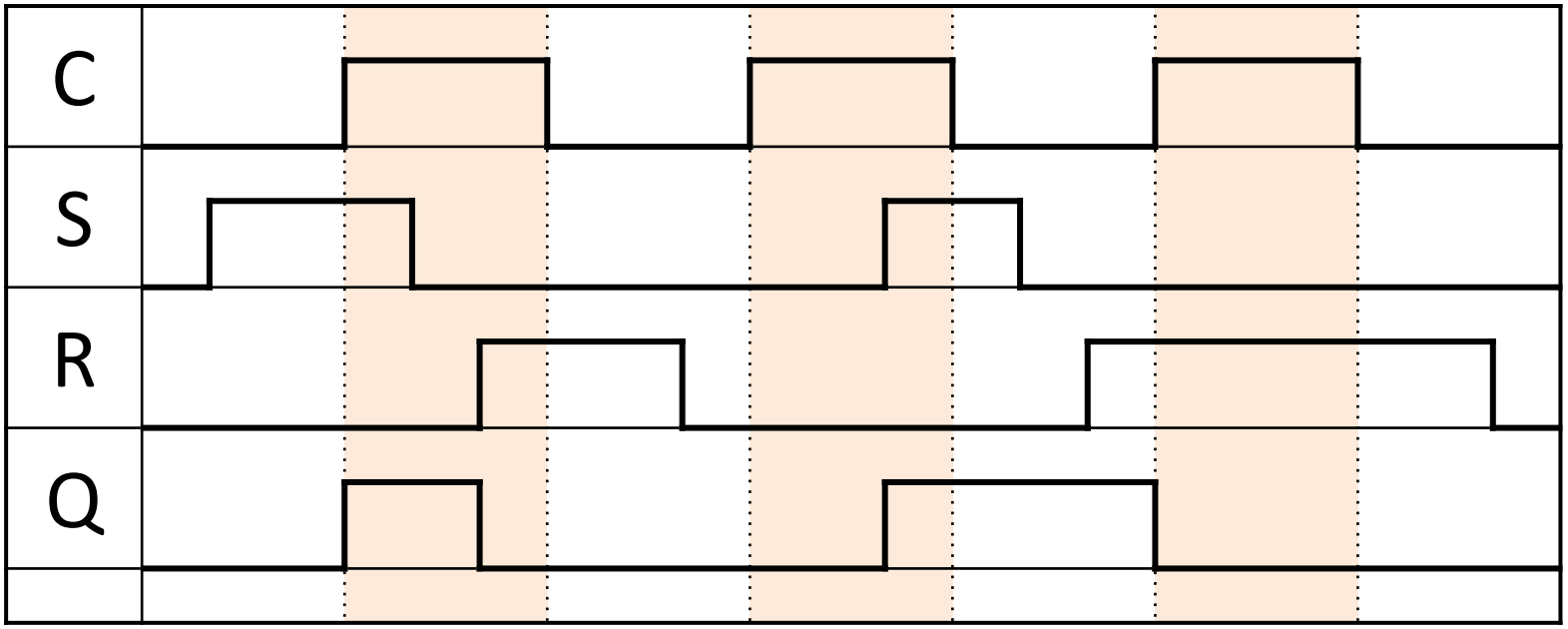
Triggers (2)

- Graphical symbols



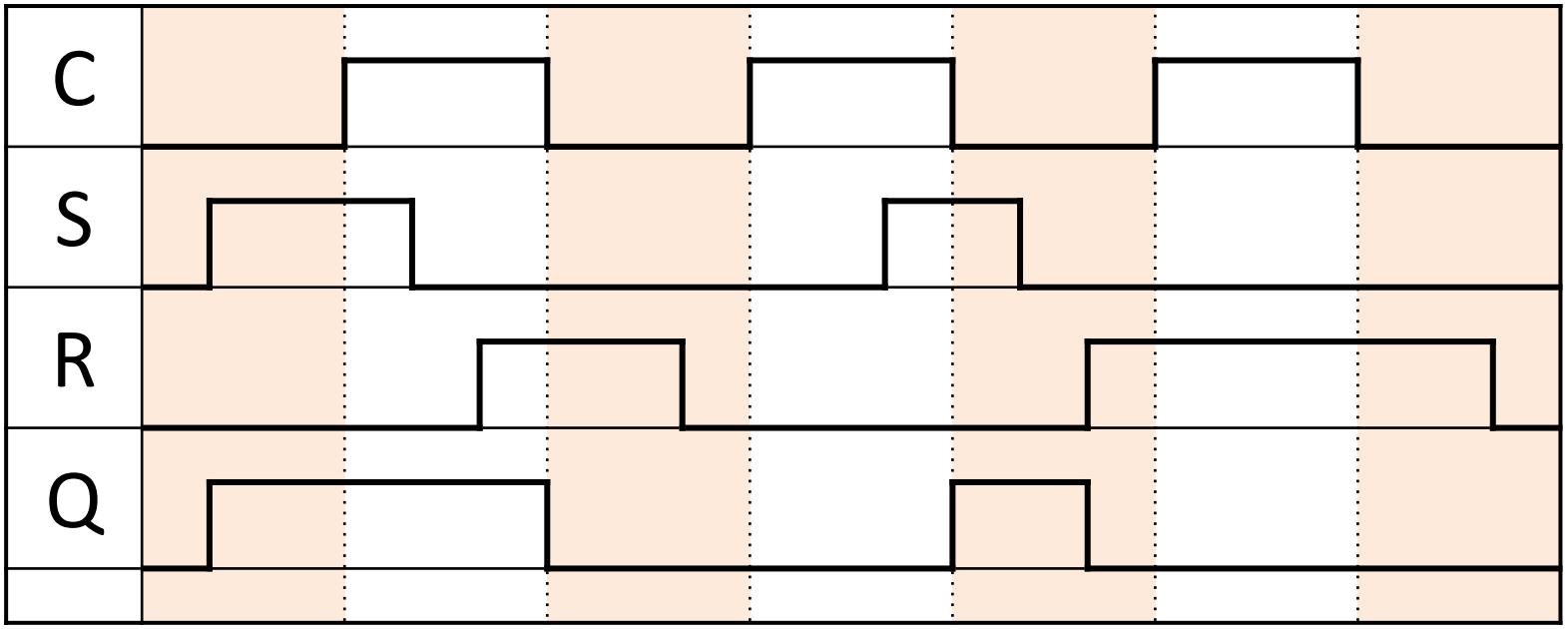
Triggers (3)

- Time diagram of a synchronous SR latch
  - Active state: level 1



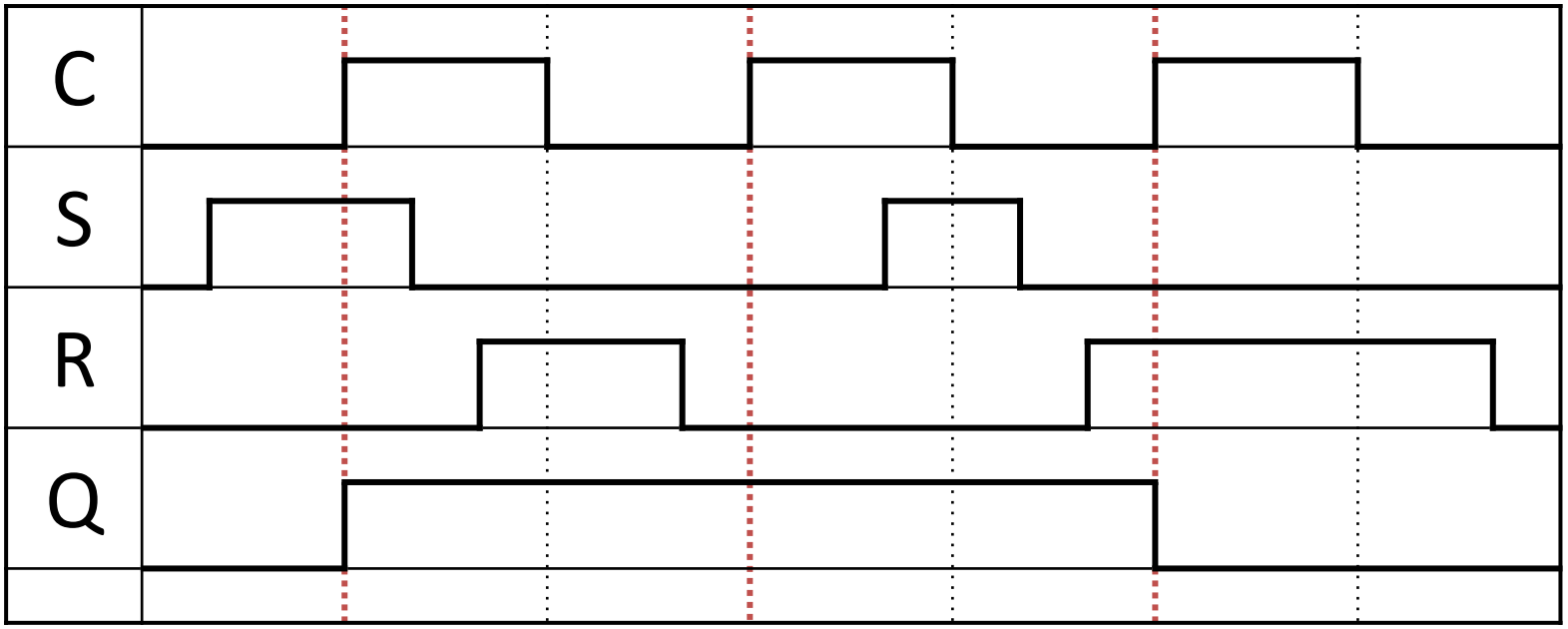
Triggers (4)

- Time diagram of a synchronous SR latch
  - Active state: level 0



Triggers (5)

- Time diagram of a synchronous SR latch
  - Active state: edge 0→1



Triggers (6)

- Time diagram of a synchronous SR latch
  - Active state: edge 1→0