

Analog-to-Digital Converter

ATxmega128A1

Networks and Embedded Software

Module 4.2.6

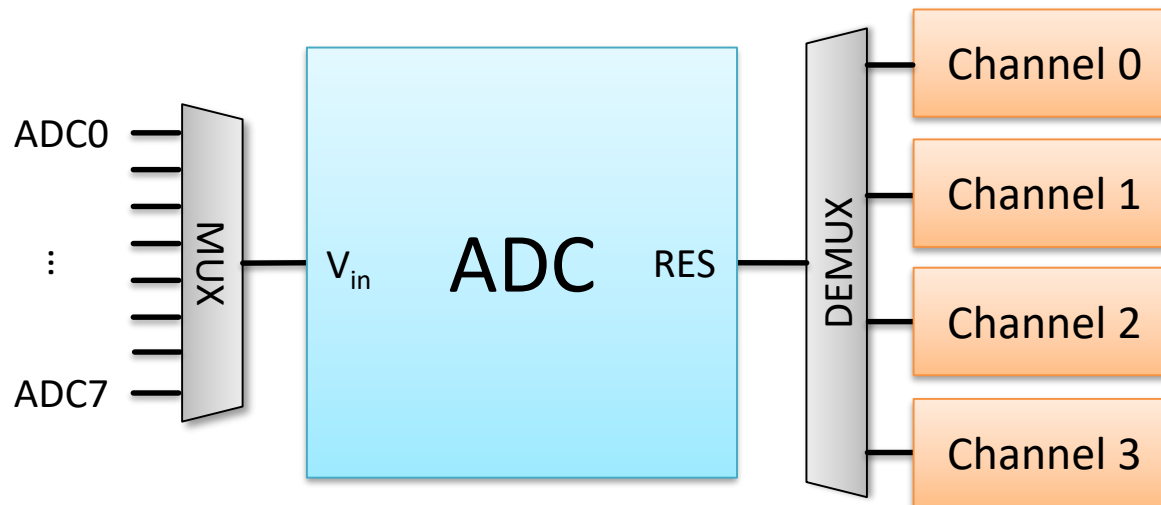
by Wolfgang Neff

ADC (1)

- Implementation
 - Two ADCs with 12-bit resolution
 - ADCA and ADCB
 - Eight analog inputs per ADC
 - ADC0 ... ADC7
 - Four channels per ADC
 - CH0, CH1, CH2, CH3
 - Selectable reference voltages
 - 1.0 V, $V_{CC}/1.6$ V, AREF (external reference)

ADC (2)

- Architecture

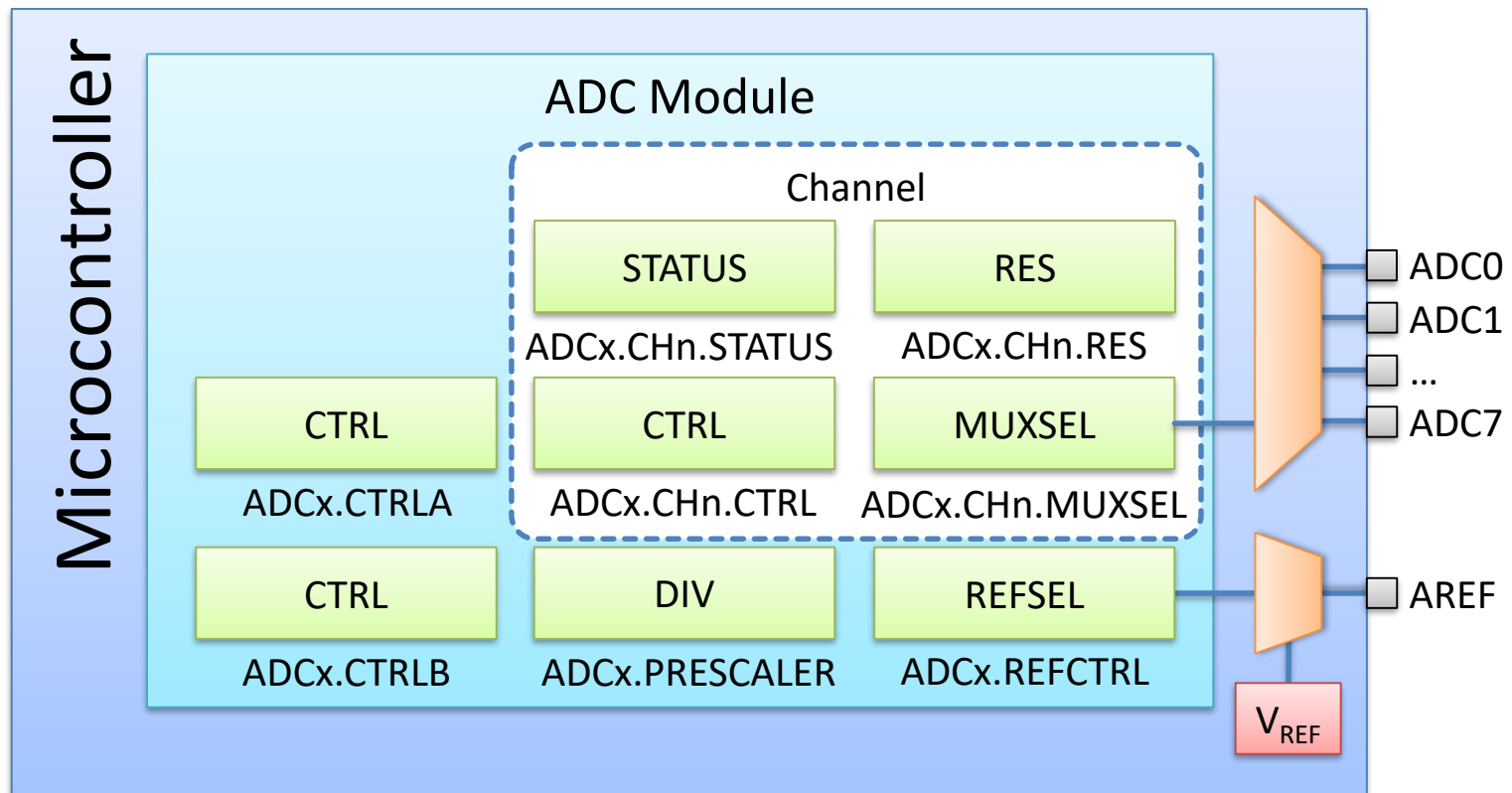


ADC (3)

- Conversion Result
 - 12-bit Resolution, Unsigned Mode
 - $RES = 4095 \cdot \frac{V_{in}}{V_{ref}} + 205$
 - Range: 0 ... 4095
 - 8-bit Resolution , Unsigned Mode
 - $RES = 255 \cdot \frac{V_{in}}{V_{ref}} + 13$
 - Range: 0 ... 255

ADC (4)

- Register Mapping



x: A,B n: 0,1,2,3

ADC (5)

- Register Description

- CTRLA: ADC Control Register A

- Bit 0 – ENABLE: ADC Enable

- CTRLB: ADC Control Register B

- Bit 4 – CONVMODE: ADC Conversion Mode

- Usually unsigned mode (default)

- Bit 3 - FREERUN: ADC Free Running Mode

- Bits 2:1 – RESOLUTION: Conversion Result Resolution

- ADC_RESOLUTION_8BIT_gc: 8-bit result

- ADC_RESOLUTION_12BIT_gc: 12-bit result

ADC (6)

- Register Description (continued)
 - PRESCALER: ADC Clock Prescaler Register
 - Bits 2:0 – PRESCALER: ADC Prescaler Configuration
 - E. g.: `ADC_PRESCALER_DIV4_gc`
 - Consult datasheet for details
 - REFCTRL: ADC Reference Control Register
 - Bits 6:4 – REFSEL: ADC Reference Selection
 - `ADC_REFSEL_INT1V_gc`: Internal 1V
 - `ADC_REFSEL_VCC_gc`: Internal VCC/1.6
 - Bit 1 – BANDGAP: Bandgap enable (for `ADC_REFSEL_INT1V_gc`)

ADC (7)

- Channel Register Description
 - RES: ADC Channel Result Register (high and low)
 - CTRL: ADC Channel Control Register
 - Bit 7 – START: START Conversion on Channel
 - Bit 1:0 – INPUTMODE: Channel Input Mode
 - Usually `ADC_CH_INPUTMODE_SINGLEENDED_gc`
 - Consult datasheet for details
 - INTFLAGS: ADC Channel Interrupt Flags Register
 - Bit 0 – IF: ADC Channel Interrupt Flag

ADC (8)

- Channel Register Description (continued)
 - INTCTRL: ADC Channel Interrupt Control Register
 - Bits 1:0 – INTLVL: ADC Interrupt Priority Level
 - ADC_CH_INTLVL_OFF_gc
 - ADC_CH_INTLVL_LO_gc
 - ...
 - MUXCTRL: ADC Channel MUX Control Register
 - Bits 6:3 - MUXPOS: Selection on Positive ADC input
 - ADC_CH_MUXPOS_PIN0_gc
 - ...

ADC (9)

- Configuration Example
 - Configure port as input
 - `PORT.DIRCLR = PIN1_bm;`
 - Configure ADC
 - `ADC.CTRLA = ADC_ENABLE_bm;`
 - `ADC.CTRLB = ADC_RESOLUTION_12BIT_gc;`
 - `ADC.REFCTRL = ADC_REFSEL_INT1V_gc |
ADC_BANDGAP_bm;`
 - `ADC.PRESCALER = ADC_PRESCALER_DIV8_gc;`

ADC (10)

- Configuration Example (continued)
 - Configure ADC Channel
 - `ADC.CH.CTRL = ADC_CH_INPUTMODE_SINGLEENDED_gc;`
 - `ADC.CH.MUXCTRL = ADC_CH_MUXPOS_PIN1_gc;`
 - Start conversion
 - `ADC.CH.CTRL |= ADC_CH_START_bm;`
 - Read result
 - `while(!(ADC.CH.INTFLAGS & ADC_CH_CHIF_bm));`
 - `result = ADCB.CH.RES;`

ADC (11)

- Register Summary

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTRLA	DMASEL[1:0]		CH[3:0]START			FLUSH	ENABLE	
CTRLB	-	-	-	CONVMODE	FREERUN	RESOLUTION[1:0]		-
REFCTRL	-	-	REFSEL[2:0]		-	-	BANDGAP	TEMPREF
EVCTRL	SWEEP[1:0]		EVSEL[2:0]			EVACT[2:0]		
PRESCALER	-	-	-	-	-	PRESCALER[2:0]		
INTFLAGS	-	-	-	-	CH[3:0]IF			
TEMP	TEMP[7:0]							
CALL	CAL[7:0]							
CALH	-	-	-	-	CAL[11:8]			

ADC (12)

- Register Summary (continued)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CHORES _L				CHORES[7:0]				
CHORES _H				CHORES[15:8]				
...				...				
CH3RES _L				CH3RES[7:0]				
CH3RES _H				CH3RES[15:8]				
CMPL				CMP[7:0]				
CMPH				CMP[15:8]				

ADC (13)

- Channel Register Summary

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTRL	START	-	-	GAIN[2:0]			INPUTMODE[1:0]	
MUXCTRL	-	MUXPOS[3:0]				-	MUXNEG[1:0]	
INTCTRL	-	-	-	-	INTMODE[1:0]		INTLVL	
INTFLAGS	-	-	-	-	-	-	-	IF
RESL	RES[7:0]							
RESH	RES[15:8]							

ADC (14)

- Interrupt Summary

Source	Description
ADCx_CH0_vect	Analog-to-digital converter channel 0 interrupt vector
ADCx_CH1_vect	Analog-to-digital converter channel 1 interrupt vector
ADCx_CH2_vect	Analog-to-digital converter channel 2 interrupt vector
ADCx_CH3_vect	Analog-to-digital converter channel 3 interrupt vector

