

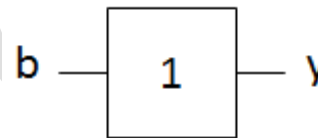
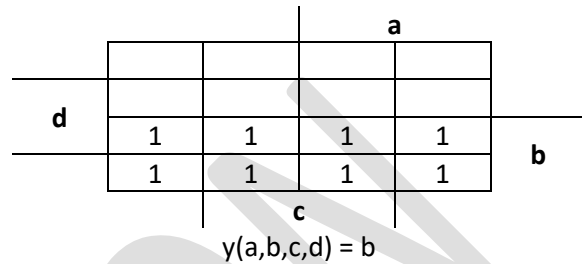
# Design of Combinatorial Circuits I

Please do the following exercises individually.

## Chip Production

a	b	c	d	y(a,b,c,d)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

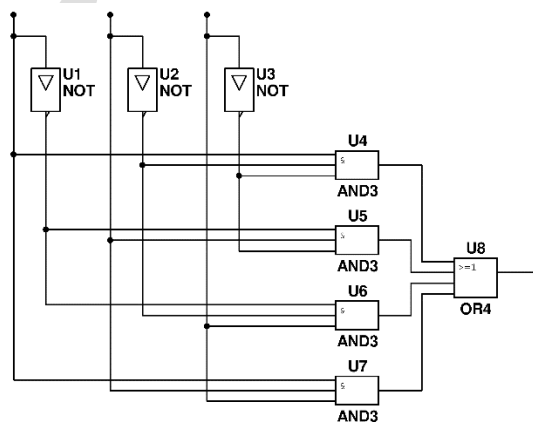
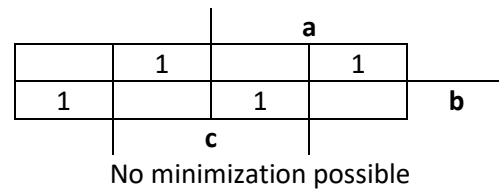
$$y(a,b,c,d) = (\neg a \wedge b \wedge \neg c \wedge \neg d) \vee (\neg a \wedge b \wedge \neg c \wedge d) \vee (\neg a \wedge b \wedge c \wedge \neg d) \vee (\neg a \wedge b \wedge c \wedge d) \vee (a \wedge b \wedge \neg c \wedge \neg d) \vee (a \wedge b \wedge \neg c \wedge d) \vee (a \wedge b \wedge c \wedge \neg d) \vee (a \wedge b \wedge c \wedge d)$$



## A XOR Gate with three Input Lines

a	b	c	$a \oplus b \oplus c$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$y(a,b,c) = (\neg a \wedge \neg b \wedge c) \vee (\neg a \wedge b \wedge \neg c) \vee (a \wedge \neg b \wedge \neg c) \vee (a \wedge b \wedge c)$$

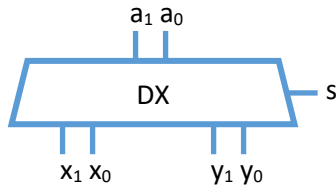


# Design of Combinatorial Circuits II

Please do the following exercises individually.

## Demultiplexer

A demultiplexer is the counterpart of a multiplexer. Look at Wikipedia<sup>1</sup> to see the interplay of a multiplexer and a demultiplexer. Please design a two bit two way demultiplexer. Look at the following graphical symbol and formal description for details.



### Formal description

$$DX: \{0,1\}^3 \mapsto \{0,1\}^4$$

$$(s, a_1, a_0) \rightarrow (x_1, x_0, y_1, y_0) := \begin{cases} (0,0, a_1, a_0) & \text{if } s = 0 \\ (a_1, a_0, 0,0) & \text{if } s = 1 \end{cases}$$

s	a <sub>1</sub>	a <sub>0</sub>	x <sub>1</sub>	x <sub>0</sub>	y <sub>1</sub>	y <sub>0</sub>
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	0	1	0
0	1	1	0	0	1	1
1	0	0	0	0	0	0
1	0	1	0	1	0	0
1	1	0	1	0	0	0
1	1	1	1	1	0	0

$$x_1(s, a_1, a_0) = (s \wedge a_1 \wedge \neg a_0) \vee (s \wedge a_1 \wedge a_0)$$

$$x_0(s, a_1, a_0) = (s \wedge \neg a_1 \wedge a_0) \vee (s \wedge a_1 \wedge a_0)$$

$$y_1(s, a_1, a_0) = (\neg s \wedge a_1 \wedge \neg a_0) \vee (\neg s \wedge a_1 \wedge a_0)$$

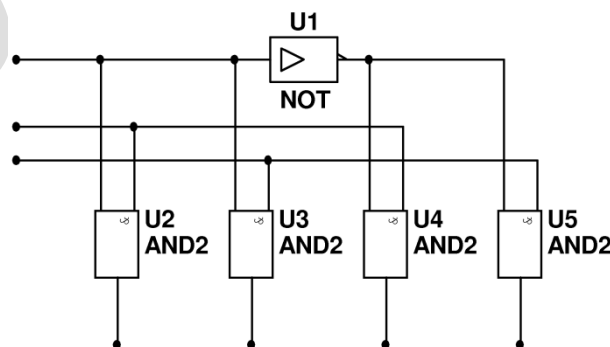
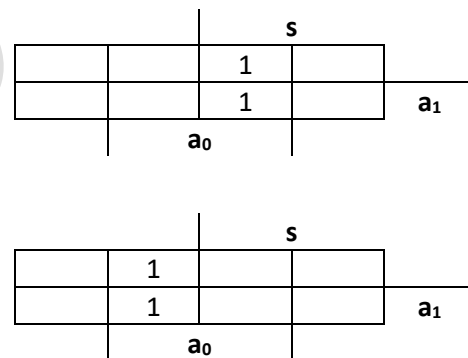
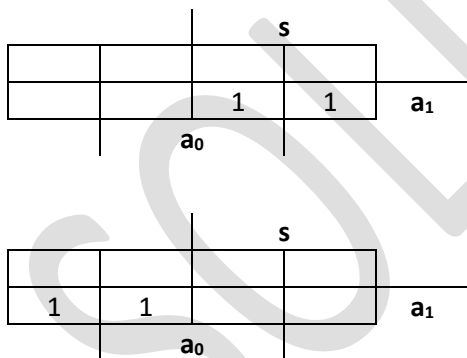
$$y_0(s, a_1, a_0) = (\neg s \wedge \neg a_1 \wedge a_0) \vee (\neg s \wedge a_1 \wedge a_0)$$

$$x_1(s, a_1, a_0) = s \wedge a_1$$

$$x_0(s, a_1, a_0) = s \wedge a_0$$

$$y_1(s, a_1, a_0) = \neg s \wedge a_1$$

$$y_0(s, a_1, a_0) = \neg s \wedge a_0$$



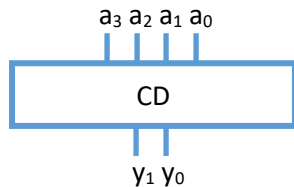
<sup>1</sup> [http://en.wikipedia.org/wiki/Demultiplexer#Cost\\_savings](http://en.wikipedia.org/wiki/Demultiplexer#Cost_savings)

# Design of Combinatorial Circuits III

Please do the following exercises individually.

## Coder

A coder tells you which line is active. An interrupt controller may use a coder. If interrupt line three is active it requests the controller to execute interrupt no 3. Please design a four bit coder. Look at the following graphical symbol and formal description for details.



### Formal description

$$CD: \{0,1\}^4 \mapsto \{0,1\}^2$$

$$(a_3, a_2, a_1, a_0) \rightarrow \begin{cases} i & \text{if only one } a_i = 1 \\ \text{undefined} & \text{otherwise} \end{cases}$$

Please remember that undefined values are don't-care terms which may help to find a better optimization.

a <sub>3</sub>	a <sub>2</sub>	a <sub>1</sub>	a <sub>0</sub>	y <sub>1</sub>	y <sub>0</sub>
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	X	X
0	1	0	0	1	0
0	1	0	1	X	X
0	1	1	0	X	X
0	1	1	1	X	X
1	0	0	0	1	1
1	0	0	1	X	X
1	0	1	0	X	X
1	0	1	1	X	X
1	1	0	0	X	X
1	1	0	1	X	X
1	1	1	0	X	X
1	1	1	1	X	X

$$y_1(a_3, a_2, a_1, a_0) = (\neg a_3 \wedge a_2 \wedge \neg a_1 \wedge \neg a_0) \vee (a_3 \wedge \neg a_2 \wedge \neg a_1 \wedge \neg a_0)$$

$$y_0(a_3, a_2, a_1, a_0) = (\neg a_3 \wedge \neg a_2 \wedge a_1 \wedge \neg a_0) \vee (a_3 \wedge \neg a_2 \wedge \neg a_1 \wedge \neg a_0)$$

