

# Inter-Integrated Circuit

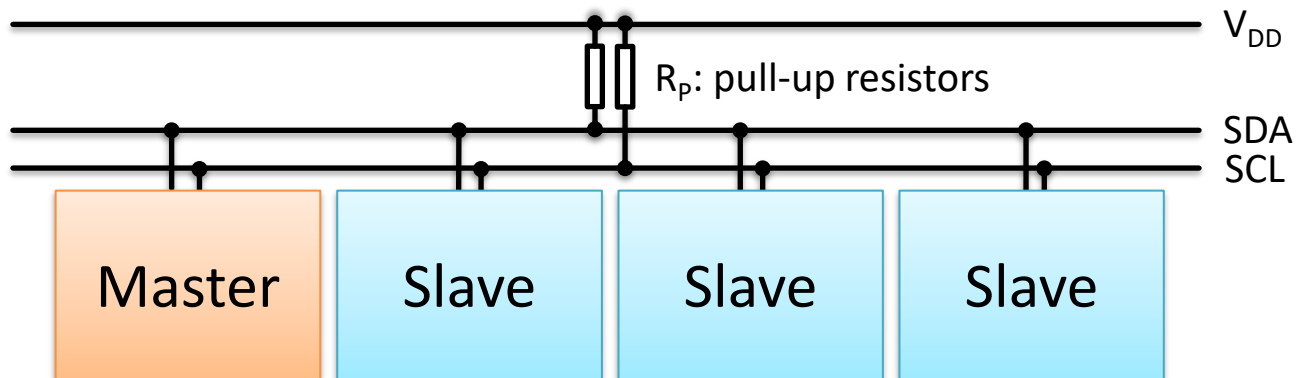
Networks and Embedded Systems

Second Grade Level

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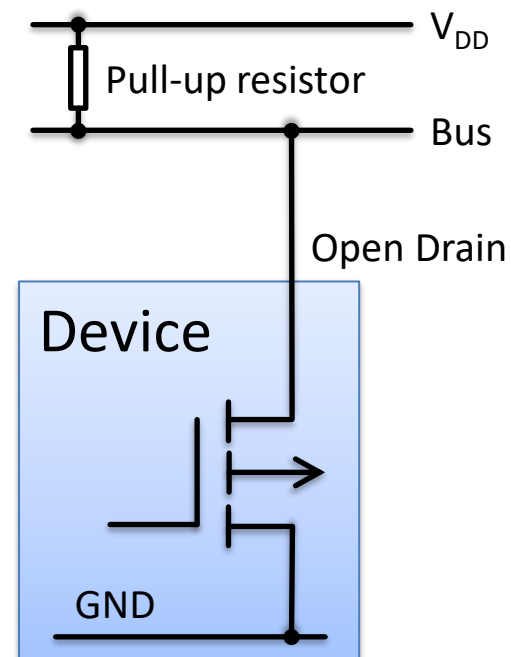
# I<sup>2</sup>C (1)

- Design
  - Two bidirectional lines
    - SDA: Serial Data Line
    - SCL: Serial Clock Line



# I<sup>2</sup>C (2)

- Design (continued)
  - Open-drain lines
    - Pulled-up resistors
    - Wired-AND
      - Dominant *0*
      - Recessive *1*
    - Collision detection



# I<sup>2</sup>C (3)

- Data Transfer

- Start Condition (S)

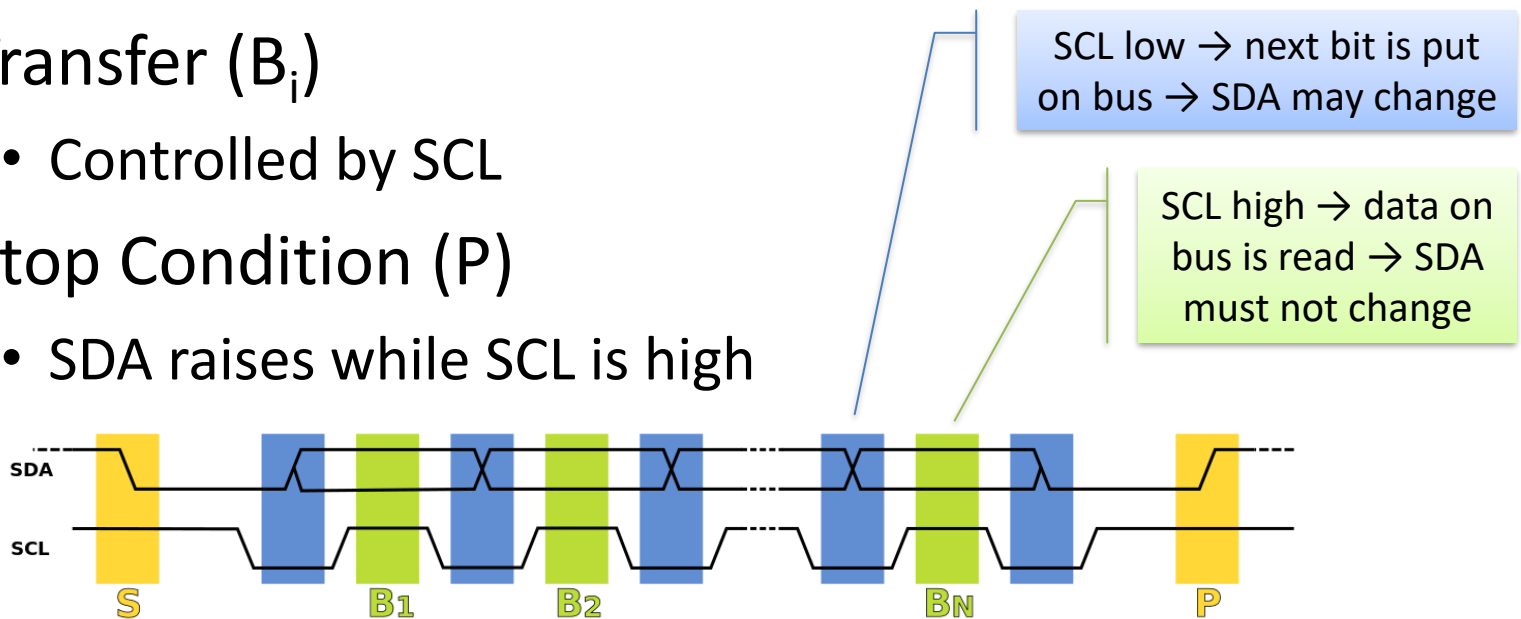
- SDA falls while SCL is high

- Transfer (B<sub>i</sub>)

- Controlled by SCL

- Stop Condition (P)

- SDA raises while SCL is high



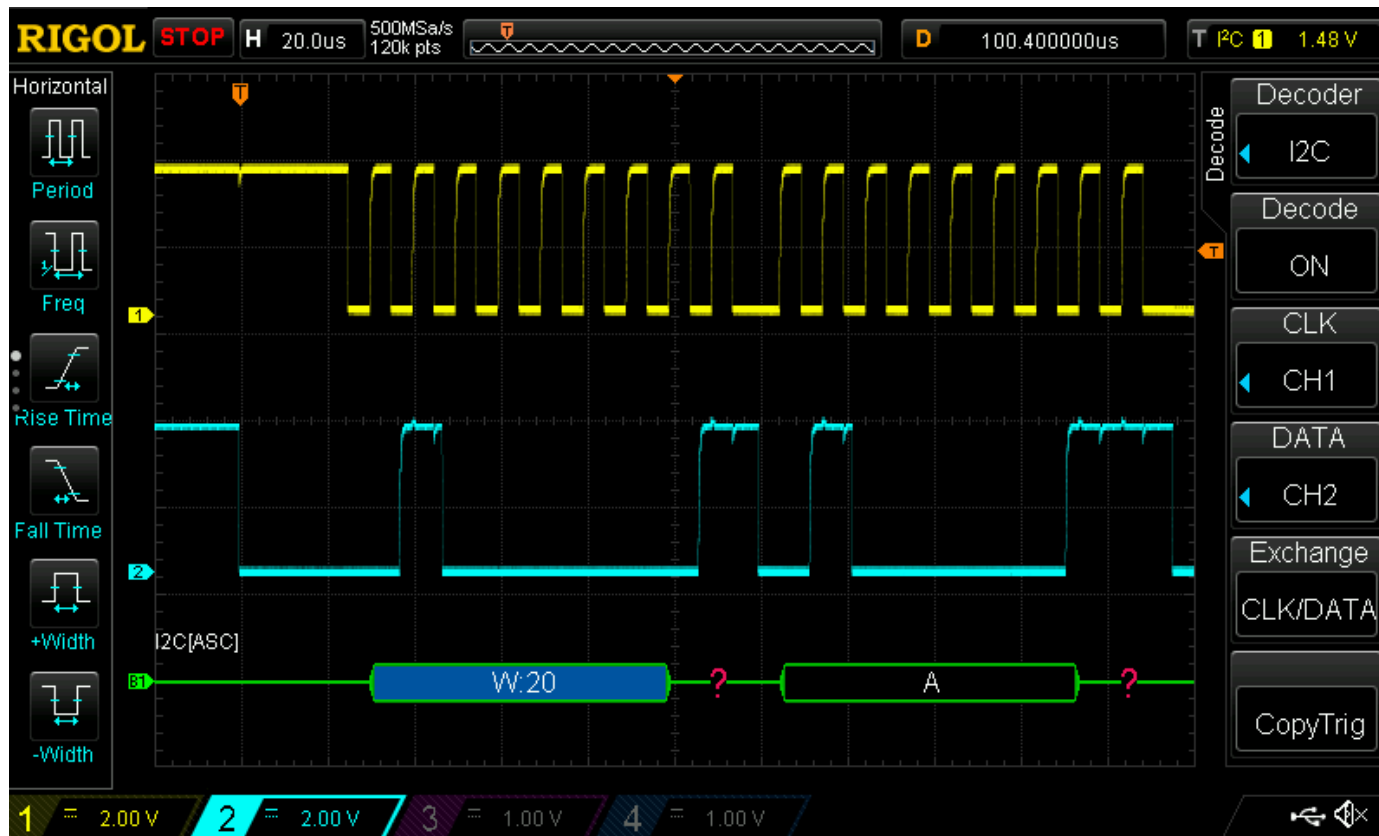
# I<sup>2</sup>C (4)

- Addressing
  - Master addresses slave
  - Address space: 7 bit (10 bit also possible)
  - First byte after start condition is address
  - Eighth bit is read/write indicator
    - 0: write, 1: read
  - Slave replies with ACK



# I<sup>2</sup>C (5)

- Real-Life Example



# I<sup>2</sup>C (6)

- Advantages
  - Just two lines necessary
  - Multiple masters possible
  - In-band addressing by protocol
  - Official I<sup>2</sup>C specifications available
  - Supports various modes of operation

# I<sup>2</sup>C (7)

- Disadvantages
  - Open-drain design increases power draw
  - Only half-duplex communication possible
  - Address conflicts
    - As slaves often restrict address space
  - No automatic bus configuration
  - Stalled slaves can produce bus faults