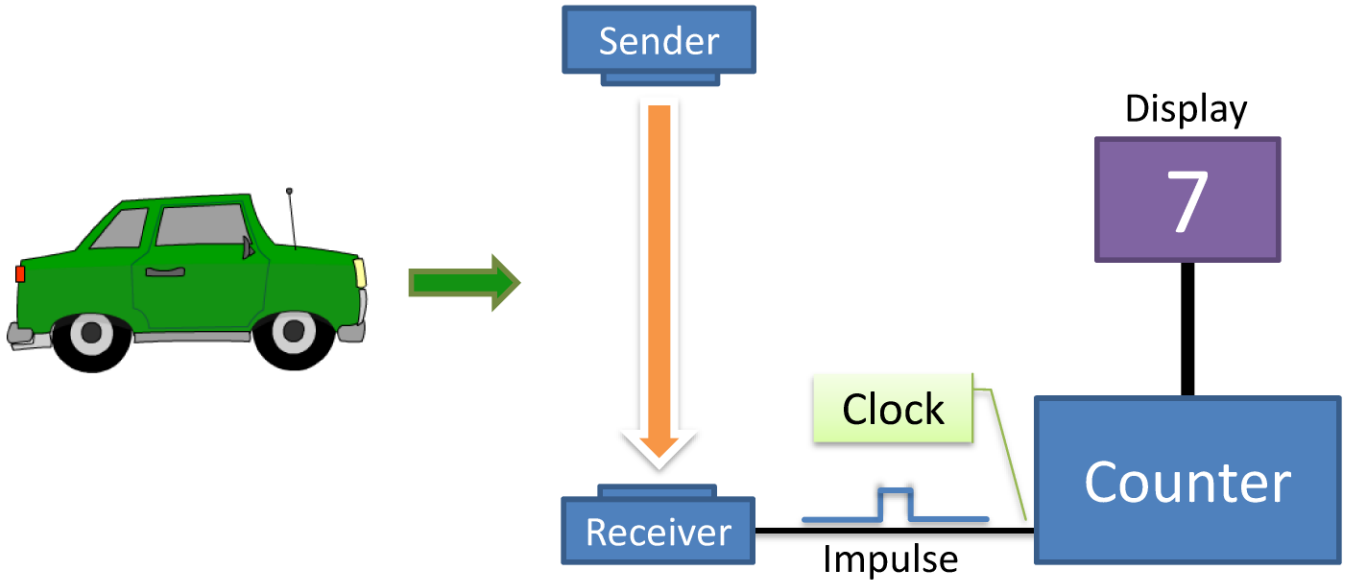
Counters

Digital Electronics

by Wolfgang Neff

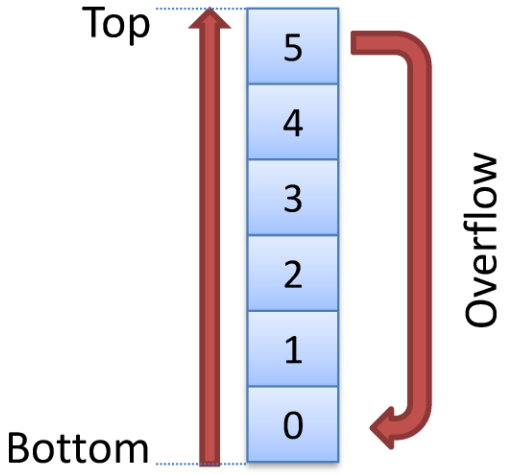
Counters (1)

- Count events
- Events are indicated by impulses



Counters (2)

- Mod-*N* counter
  - Counter have a range
    - 0 … N-1 (0 … 5)
  - Counter overflow
    - N-1 → 0 (0, 1, 2, 3, 4, 5, 0, 1, …)
  - Modulo
    - Remainder of division
      - 5 mod 6 = 5
      - 6 mod 6 = 0
      - 7 mod 6 = 1

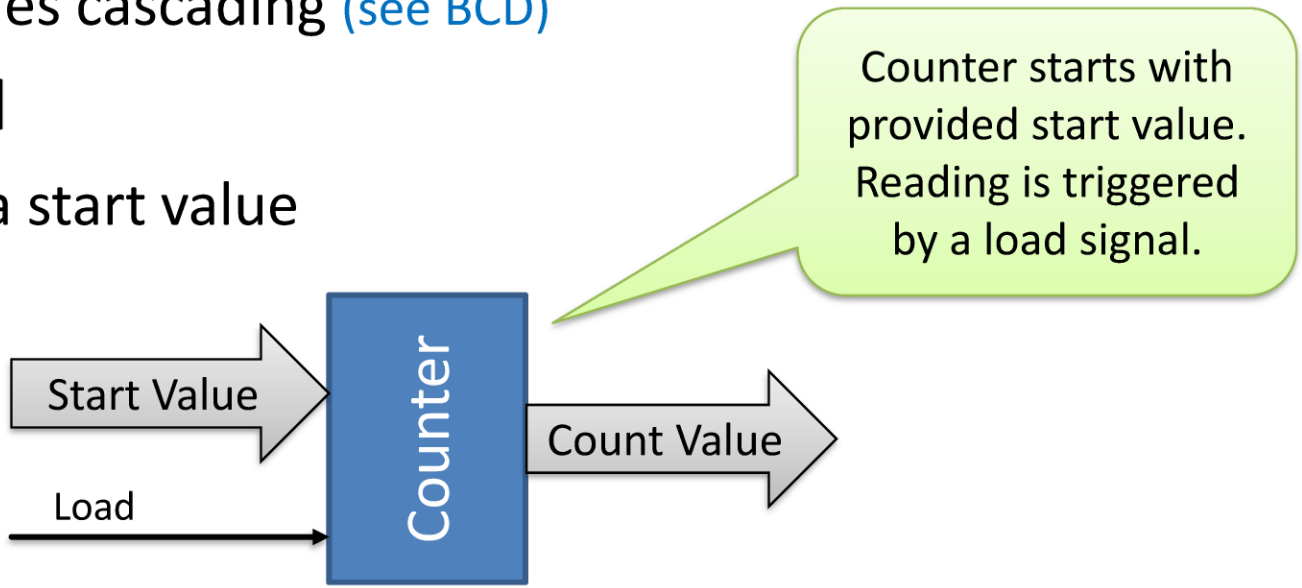


Counters (3)

- Features
  - Enable
    - Enables or disables clock
  - Reset
    - Resets counter value
  - Up/down
    - Changes the counting direction
      - Countdown

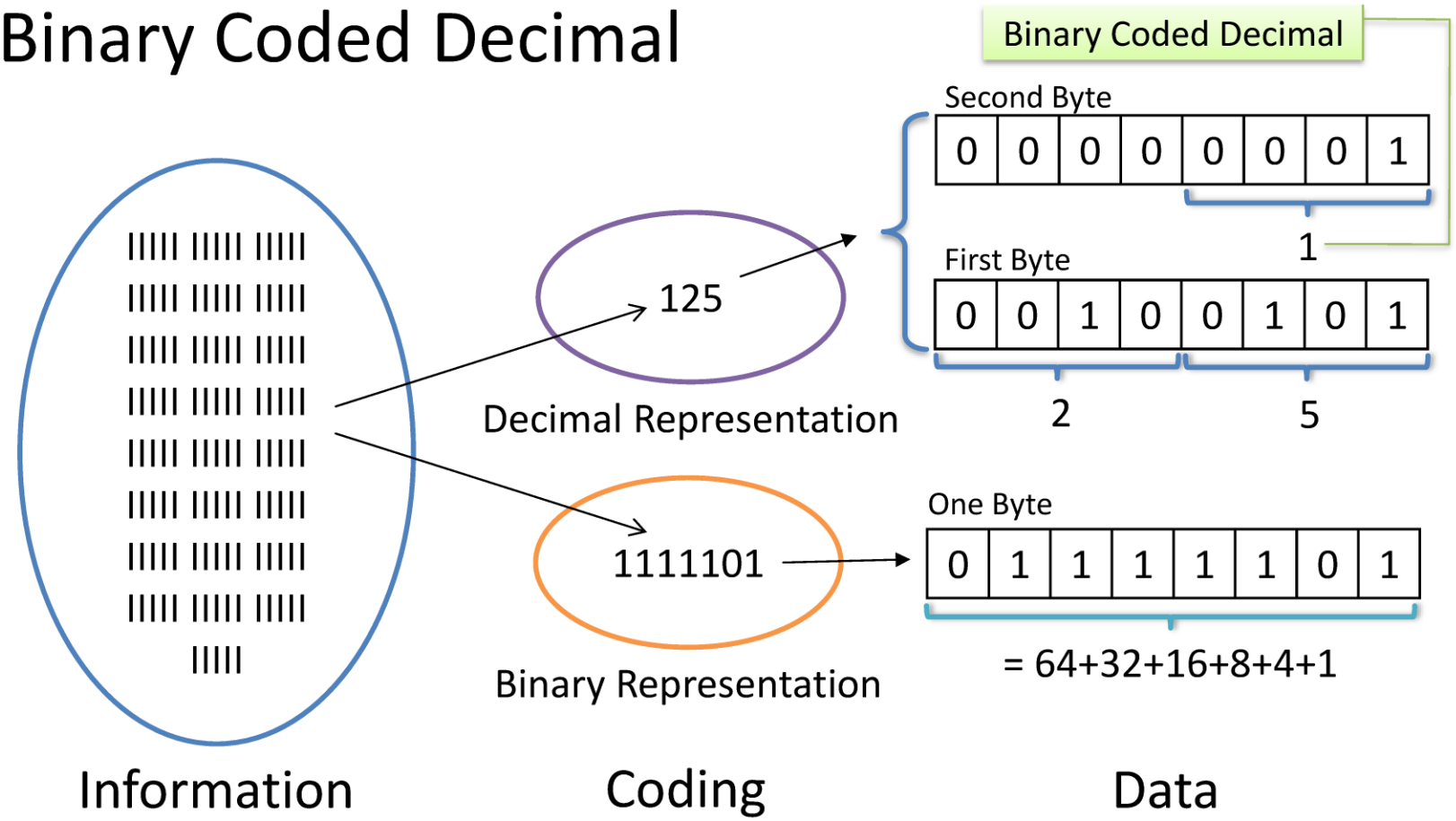
Counters (4)

- Features (continued)
  - Overflow Indicator
    - Enables cascading (see BCD)
  - Preload
    - Sets a start value



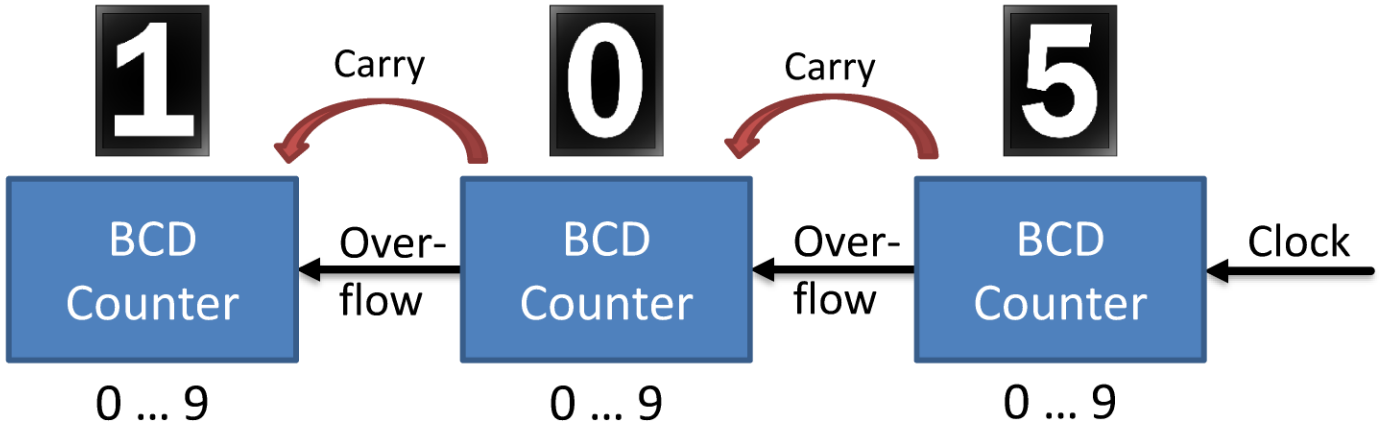
BCD (1)

- Binary Coded Decimal



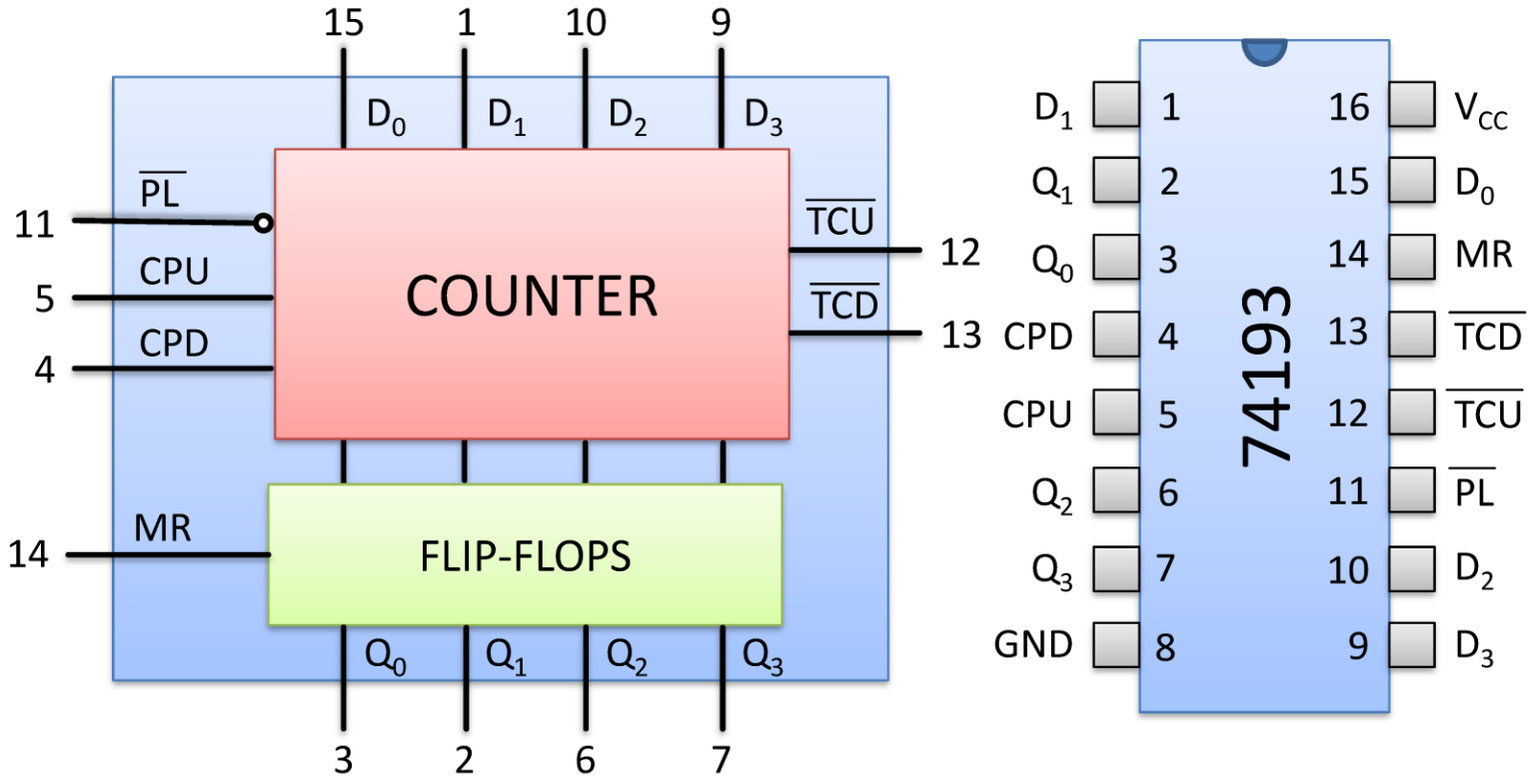
BCD (2)

- BCD Counter (mod-10 counter)
- Position Cascading
  - Odometer (Mileage counter)



Counters (5)

- 74193 – 4-bit binary up/down counter



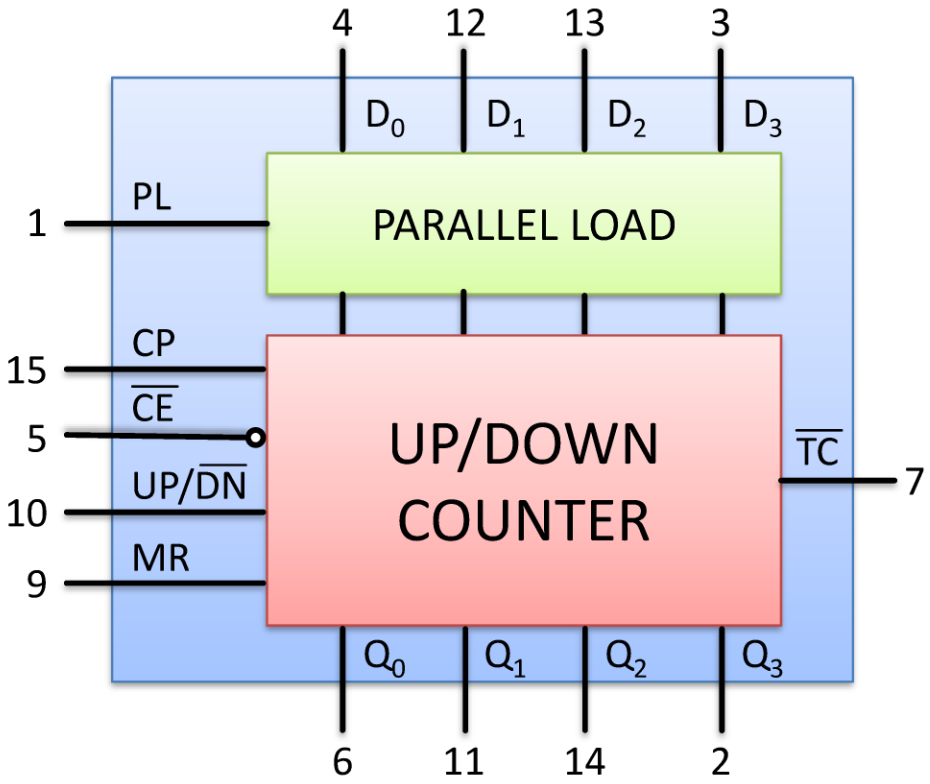
Counters (6)

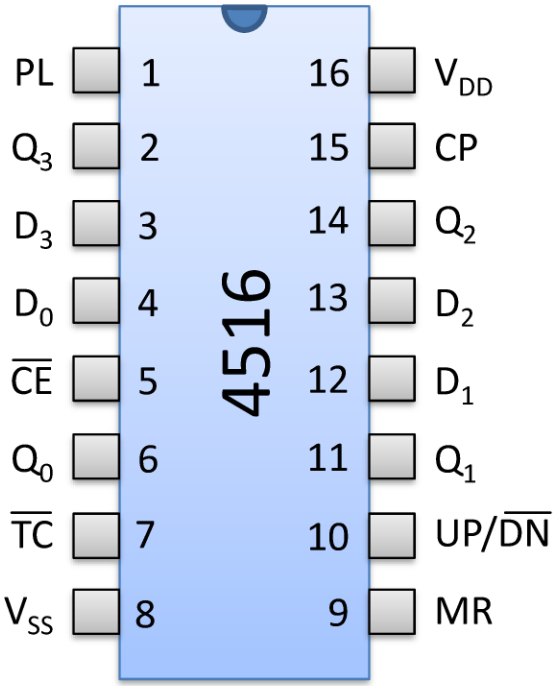
- 74193 – 4-bit binary up/down counter (continued)

Symbol	Pin	Description
D_0, D_1, D_2, D_3	15, 1, 10, 9	data input
Q_0, Q_1, Q_2, Q_3	3, 2, 6, 7	flip-flop output
CPD	4	count down clock input; L-to-H
CPU	5	count up clock input; L-to-H
GND	8	ground (0 V)
$\overline{PL}$	11	asynchronous parallel load input
$\overline{TCU}$	12	terminal count up (carry) output
$\overline{TCD}$	13	terminal count down (carry) output
MR	14	asynchronous master reset input
V_{CC}	16	supply voltage

Counters (7)

- 4516 – Binary up/down counter





Counters (8)

- 4516 – Binary up/down counter (continued)

Symbol	Pin	Description
PL	1	parallel load input
D_0, D_1, D_2, D_3	4, 12, 13, 3	parallel input
$\overline{CE}$	5	count enable input
Q_0, Q_1, Q_2, Q_3	6, 11, 14, 2	parallel output
V_{SS}	8	ground
$\overline{TC}$	7	terminal count output
MR	9	master reset input
UP/$\overline{DN}$	10	up/down count control input
CP	15	clock pulse input
V_{DD}	16	supply voltage