Interrupts

ATmega1284P

Networks and Embedded Software

Module 4.3.2

by Wolfgang Neff

Interrupts (1)

- Overview
  - Enabling Interrupts Globally
    - Set bit in CPU status register
    - Built-in interrupt enabling functions
      - `sei(); // set the global interrupt flag`
      - `cli(); // clear the global interrupt flag`
  - Interrupt Priority Levels
    - There are no interrupt priority levels
  - Declarations of Interrupt Service Routines
    - ISR(*VECTOR*) { … }

Interrupts (2)

- Register Description
  - SREG: Status Register
    - Bit 7 – I: Global Interrupt Enable
  - MCU: MCU Register
    - Bit 1 – IVSEL: Interrupt Vector Select
    - Bit 0 – IVCE: Interrupt Vector Change Enable

Interrupts (3)

- Example: USART Receive Complete Interrupt
  - Implement interrupt service routine
    - `ISR(USART1_RXC_vect) { … }`
  - Enable device interrupt
    - `UCSR1B |= (1 << RXCIE1);`
  - Enable global interrupts
    - `sei();`

Interrupts (4)

- SREG Register Summary

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SREG	**I**	T	H	S	V	N	Z	C

Interrupts (5)

- MCU Register Summary

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MCUCR	JDT	BODS	BODSE	PUD	-	-	IVSEL	IVCE