# Interrupts

## ATmega4809

Networks and Embedded Software

Module 4.3.2

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# Interrupts (1)

- Implementation
  - Enabling Interrupts Globally
    - Set bit in CPU status register
    - Built-in interrupt enabling functions
      - `sei(); // set the global interrupt flag`
      - `cli(); // clear the global interrupt flag`
  - Interrupt Priority Levels
    - Three priority levels
      - NMI, Level 1, Level 0

# Interrupts (2)

- Implementation (continued)
  - Interrupt Priority Levels (continued)
    - Handled by CPUINT
      - CPU Interrupt Controller
    - One vector is selectable as level 1
  - Declarations of Interrupt Service Routines
    - ISR(*VECTOR*) { … }
    - Interrupt flag must be cleared in ISR
      - This is done by writing a '1' to its bit position

# Interrupts (3)

- Register Description
  - SREG: Status Register
    - Bit 7 – I: Global Interrupt Enable
  - CPUINT.LVL1VEC: Priority Level 1 Register
    - Bit 7:0 – LVL1VEC: Interrupt Vector with Priority Level 1

# Interrupts (4)

- Example: USART Receive Complete Interrupt
  - Implement interrupt service routine
    - ```
      ISR(USART_RXC_vect) {
          …
          // Clear interrupt flag
          USART.STATUS |= USART_RXCIE_bm;
      }
      ```
  - Enable device interrupt
    - `USART.CTRLA |= USART_RXCIE_bm;`
  - Enable global interrupts
    - `CPU_SREG |= CPU_I_bm;`
      ```

# Interrupts (5)

- SREG Register Summary

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| **SREG** | **I** | T | H | S | V | N | Z | C |

# Interrupts (6)

- CPUINT Register Summary

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| CTRLA | - | IVSEL | CVT | - | - | - | - | LVL0RR |
| STATUS | NMIEX | - | - | - | - | - | LVL1EX | LVL0EX |
| LVL0PRI | LVL0PRI[7:0] | | | | | | | |
| **LVL1VEC** | **LVL1VEC[7:0]** | | | | | | | |