Timers

ATmega4809

Networks and Embedded Software

Module 4.3.4

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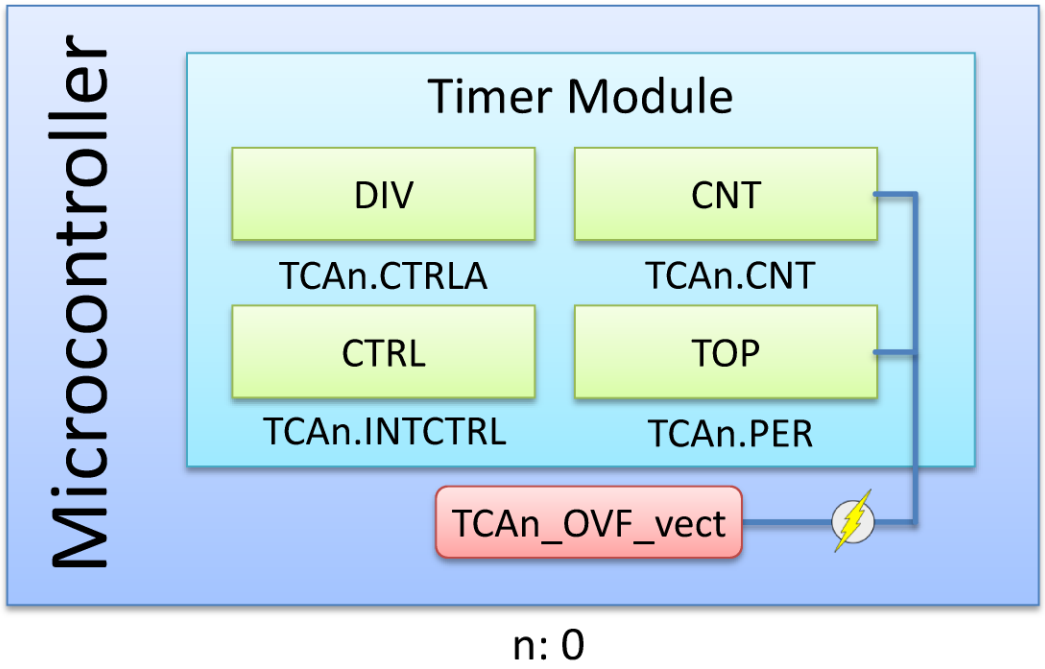
Timers (1)

- Implementation
  - One 16-bit timer/counter type A
    - Timer Period Register
    - Three Compare Channels
    - Waveform Generation (pulse-width modulation)
    - Normal and Split Mode (two 8-bit timer/counters)
  - Four 16-bit timer/counter type B
    - Periodic Interrupt Generation
    - 8-bit Pulse-Width Modulation

Timers (2)

- Register Mapping (type A, normal mode)



Timers (3)

- Register Description
  - CNT: Counter Register (high and low byte)
  - PER: Period Register (high and low byte)
  - INTCTRLA: Interrupt Enable Register A
    - Bit 0 – OVF: Timer Overflow Interrupt Enable
      - `TCA_SINGLE_OVF_bm`: enable interrupt
    - Bit 6:4 – CMPn: Compare Channel n Interrupt Enable
      - `TCA_SINGLE_CMP0_bm`: enable channel 0 interrupt
      - `TCA_SINGLE_CMP1_bm`: enable channel 1 interrupt
      - `TCA_SINGLE_CMP2_bm`: enable channel 2 interrupt

Timers (4)

- Register Description (continued)
  - CTRLA: Control Register A
    - Bit 0 – ENABLE: Timer Enable
      - `TCA_SINGLE_ENABLE_bm`: enable timer
    - Bit 3:1 – CLKSEL: Clock Select
      - `TCA_SINGLE_CLKSEL_DIV1_gc`: no prescaling
      - `TCA_SINGLE_CLKSEL_DIV2_gc`: prescaler is 2
      - `TCA_SINGLE_CLKSEL_DIV4_gc`: prescaler is 4
      - …
      - `TCA_SINGLE_CLKSEL_DIV1024_gc`: prescaler is 1024

Timers (5)

- Configuration Example
  - Normal mode, Prescaler=8, PER = 24999
  - Enable Timer and Set Prescaler
    - `TIMER.SINGLE.CTRLA = TCA_SINGLE_CLKSEL_DIV8_gc | TCA_SINGLE_ENABLE_bm;`

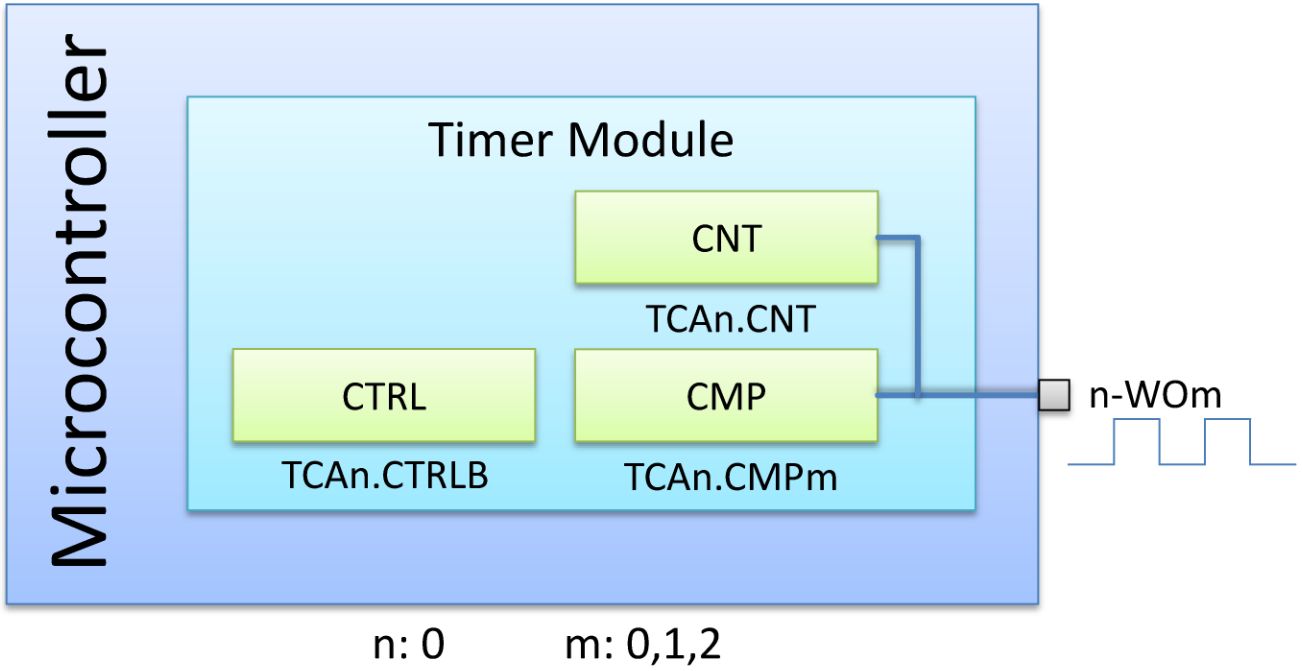
SINGLE means normal mode

Timers (6)

- Configuration Example (continued)
  - Set period
    - `TIMER.SINGLE.PER = 24999;`
  - Enable interrupt
    - `TIMER.SINGLE.INTCTRL = TCA_SINGLE_OVF_bm;`
  - Implement interrupt
    - `ISR(TIMER_OVF_vect) { … }`

PWM (1)

- Register Mapping (type A, normal mode)



PWM (2)

- Register Description
  - CTRLB: Control Register B
    - Bit 6 – CMP2EN: Compare Register 2 Enable
    - Bit 5 – CMP1EN: Compare Register 1 Enable
    - Bit 4 – CMP0EN: Compare Register 0 Enable
    - Bit 2:0 – WGMODE: Waveform Generation Mode
      - Usually `TC_WGMODE_SS_gc`: Single-Slope PWM
      - Consult datasheet for details

PWM (3)

- Register Description (continued)
  - CMP0 - Compare Register 0 (high and low)
  - CMP1 - Compare Register 1 (high and low)
  - CMP2 - Compare Register 2 (high and low)

PWM (4)

- Configuration Example (50% duty cycle)
  - Configure PWM output pin
    - `PORT.DIR |= PIN0_bm;`
  - Configure timer
    -
```
PWM.SINGLE.CTRLA =
      TCA_SINGLE_CLKSEL_DIV2_gc |
      TCA_SINGLE_ENABLE_bm;
```

PWM (5)

- Configuration Example (continued)
  - Enable single-slope PWM
    - `PWM.SINGLE.CTRLB = TCA_SINGLE_CMP0EN_bm | TCA_SINGLE_WGMODE_SINGLESLOPE_gc;`
  - Set period and compare value
    - `PWM.SINGLE.CMP0 = 5000;`
    - `PWM.SINGLE.PER = 10000;`

Timers (7)

- Register Summary (type A, normal mode)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTRLA	-	-	-	-	**CLKSEL**			**ENABLE**
CTRLB	-	**CMP2EN**	**CMP1EN**	**CMP0EN**	ALUPD	**WGMODE**		
CTRLC	-	-	-	-	-	CMP2OV	CMP1OV	CMP0OV
CTRLD	-	-	-	-	-	-	-	SPLITM
CTRLECLR	-	-	-	-	CMD[1:0]		LUPD	DIR
CTRLESET	-	-	-	-	CMD[1:0]		LUPD	DIR
CTRLFCCLR	-	-	-	-	CMP2BV	CMP1BV	CMP0BV	PERBV
CTRLFSET	-	-	-	-	CMP2BV	CMP1BV	CMP0BV	PERBV

Timers (8)

- Register Summary (continued)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EVCTRL	-	-	-	-	EVACT[1:0]			CNTEI
INTCTRL	-	CMP2	CMP1	CMP0	-	-	-	OVF
INTFLAGS	-	CMP2	CMP1	CMP0	-	-	-	OVF
DBGCTRL	-							DGBRUN
TEMP	TEMP[7:0]							
CNTL	CNT[7:0]							
CNTH	CNT[15:8]							

Timers (9)

- Register Summary (finished)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PERL	PER[7:0]							
PERH	PER[15:8]							
CMP0L	CMP[7:0]							
CMP0H	CMP[15:8]							
CMP1L	CMP[7:0]							
CMP1H	CMP[15:8]							
CMP2L	CMP[7:0]							
CMP2H	CMP[15:8]							

Timers (10)

- Interrupt Summary

Source	Description
TCAn_OVF_vect	Timer/Counter overflow interrupt vector
TCAn_CMP0_vect	Timer/Counter compare channel 0 interrupt vector
TCAn_CMP1_vect	Timer/Counter compare channel 1 interrupt vector
TCAn_CMP2_vect	Timer/Counter compare channel 2 interrupt vector