

Timers

ATxmega128A1

Networks and Embedded Software

Module 4.3.4

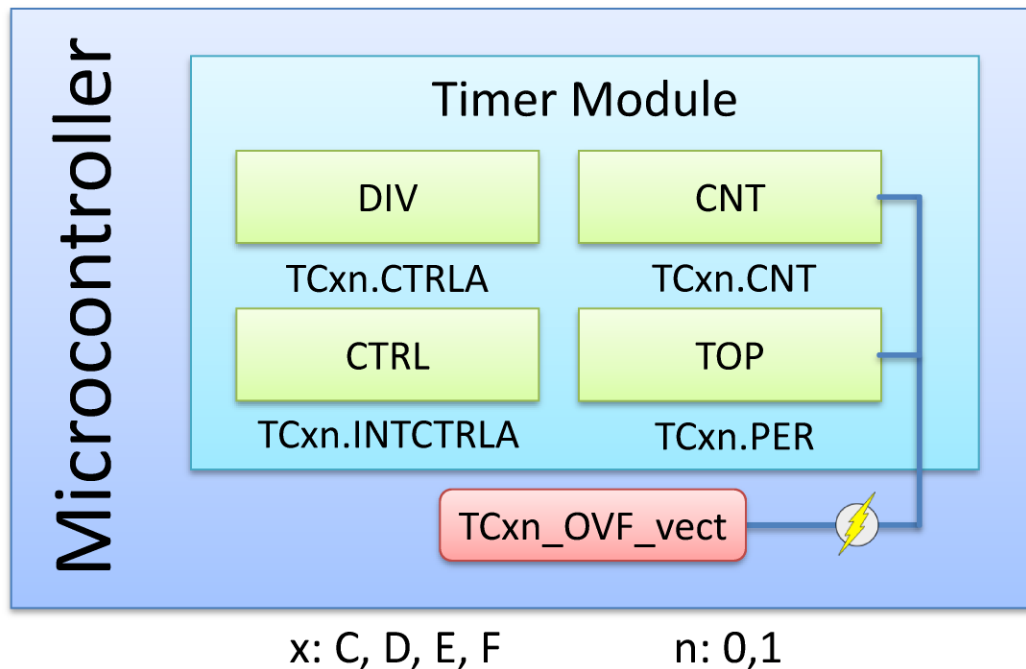
by Wolfgang Neff

Timers (1)

- Implementation
 - Eight 16-bit timer/counter modules
 - Two timer modules per port
 - Type 0: TCC0, TCD0, TCE0, TCF0
 - Type 1: TCC1, TCD1, TCE1, TCF1
 - Four or two compare registers
 - Type 0: four compare registers
 - Type 1: two compare registers

Timers (2)

- Register Mapping



Timers (3)

- Register Description
 - CNT: Counter Register (high and low byte)
 - PER: Period Register (high and low byte)
 - INTCTRLA: Interrupt Enable Register A
 - Bit 1:0 – OVFINTLVL: Timer Overflow Interrupt Level
 - TC_OVFINTLVL_OFF_gc: interrupt disabled
 - TC_OVFINTLVL_LO_gc: low level interrupt
 - TC_OVFINTLVL_MED_gc: medium level interrupt
 - TC_OVFINTLVL_HI_gc: high level interrupt

Timers (4)

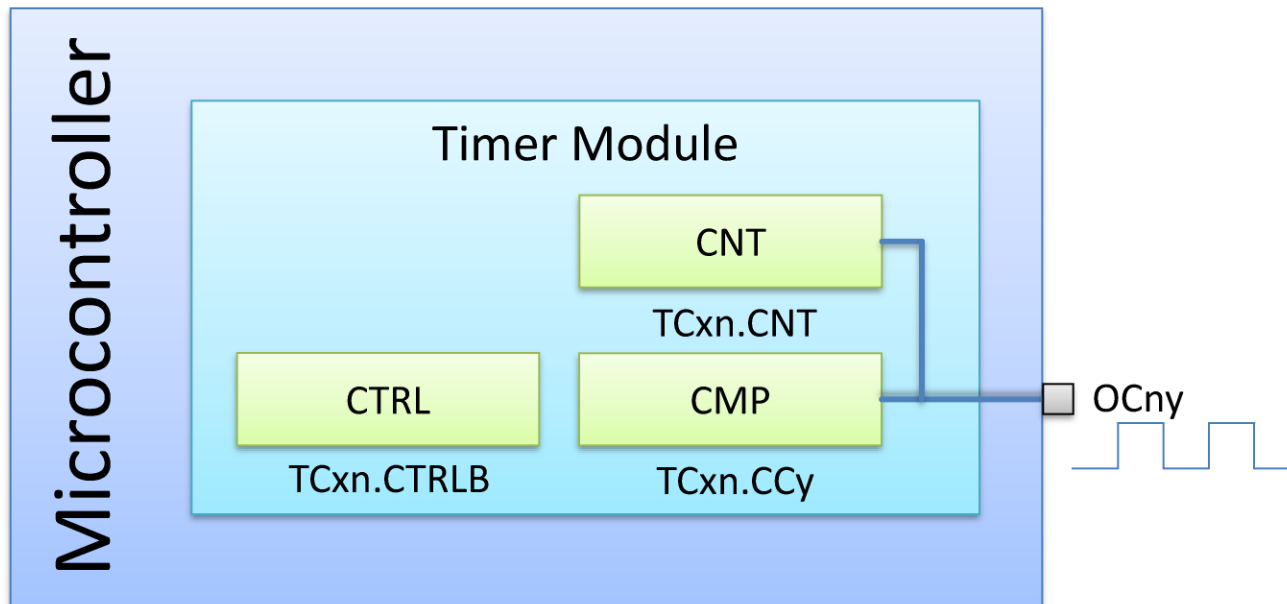
- Register Description (continued)
 - CTRLA: Control Register A
 - Bit 3:0 – CLKSEL: Clock Select
 - TC_CLKSEL_OFF_gc: timer is off
 - TC_CLKSEL_DIV1_gc: no prescaling
 - TC_CLKSEL_DIV2_gc: prescaler is 2
 - TC_CLKSEL_DIV4_gc: prescaler is 4
 - TC_CLKSEL_DIV8_gc: prescaler is 8
 - TC_CLKSEL_DIV64_gc: prescaler is 64
 - TC_CLKSEL_DIV256_gc: prescaler is 256
 - TC_CLKSEL_DIV1024_gc: prescaler is 1024

Timers (5)

- Configuration Example (prescaler=8, PER = 24999)
 - Set prescaler
 - `TIMER.CTRLA = TC_CLKSEL_DIV8_gc;`
 - Set period
 - `TIMER.PER = 24999;`
 - Enable interrupt
 - `TIMER.INTCTRLA = TC_OVFINTLVL_LO_gc;`
 - Implement interrupt
 - `ISR(TIMER_OVF_vect) { ... }`

PWM (1)

- Register Mapping



x: C, D, E, F n: 0,1 y: A, B, (if n = 0 also C, D)

PWM (2)

- Register Description
 - CTRLB: Control Register B
 - Bit 7 – CCDEN: Compare or Capture Enable
 - Bit 6 – CCCEN: Compare or Capture Enable
 - Bit 5 – CCBEN: Compare or Capture Enable
 - Bit 4 – CCAEN: Compare or Capture Enable
 - Bit 2:0 – WGMODE: Waveform Generation Mode
 - Usually `TC_WGMODE_SS_gc`: Single-Slope PWM
 - Consult datasheet for details

PWM (3)

- Register Description (continued)
 - CCA: Compare or Capture Register A (high and low)
 - CCB: Compare or Capture Register B (high and low)
 - CCC: Compare or Capture Register C (high and low)
 - CCD: Compare or Capture Register D (high and low)

PWM (4)

- Configuration Example (50% duty cycle)
 - Configure PWM output pin
 - `PORT.DIR |= PIN0_bm;`
 - Configure timer and enable single-slope PWM
 - `PWM.CTRLA = TC_CLKSEL_DIV2_gc;`
 - `PWM.CTRLB = TC0_CCAEN_bm | TC_WGMODE_SS_gc;`
 - Set period and compare value
 - `PWM.CCA = 5000;`
 - `PWM.PER = 10000;`

Timers (6)

- Register Summary

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTRLA	-	-	-	-	CLKSEL			
CTRLB	CCDEN	CCCEN	CCBEN	CCAEN	-	WGMODE[2:0]		
CTRLC	-	-	-	-	CMPC	CMPC	CMPB	CMPA
INTCTRLA					ERRINTLVL[1:0]		OVINTLVL[1:0]	
INTCTRLB	CCDINTLVL[1:0]		CCCINTLVL[1:0]		CCBINTLVL[1:0]		CCAINTLVL[1:0]	
INTFLAGS	CCDIF	CCCIF	CCBIF	CCAIF			ERRIF	OVFIF
CNTL	CNT[7:0]							
CNTH	CNT[15:8]							

Timers (7)

- Register Summary (continued)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PERL	PER[7:0]							
PERH	PER[15:8]							
CCAL	CCA[7:0]							
CCAH	CCA[15:8]							
...	...							
CCDL	CCD[7:0]							
CCDH	CCD[15:8]							

Timers (8)

- Interrupt Summary

Source	Description
TCxn_OVF_vect	Timer/Counter overflow interrupt vector
TCxn_ERR_vect	Timer/Counter error interrupt vector
TCxn_CCA_vect	Timer/Counter compare or capture channel A interrupt vector
TCxn_CCB_vect	Timer/Counter compare or capture channel B interrupt vector
TCxn_CCC_vect	Timer/Counter compare or capture channel C interrupt vector
TCxn_CCD_vect	Timer/Counter compare or capture channel D interrupt vector