# Analog-to-Digital Converter

## ATmega1284P

Networks and Embedded Software

Module 4.2.6

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# ADC (1)

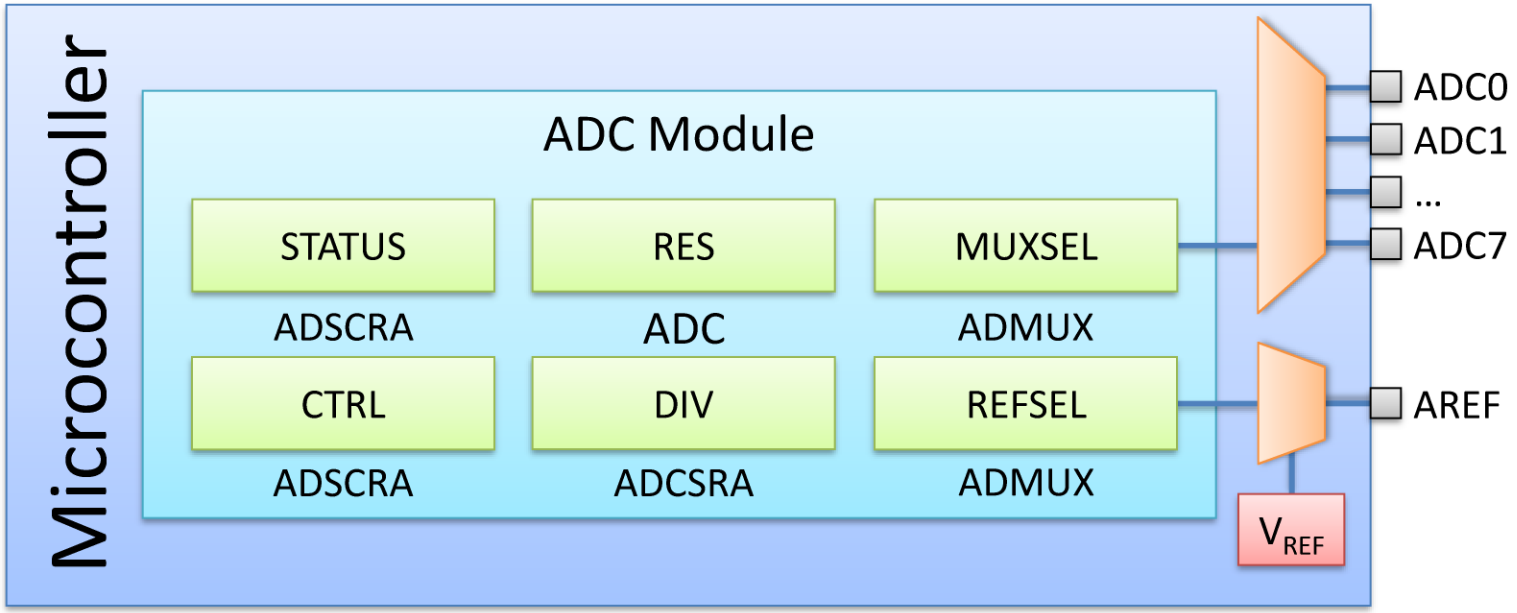
- Implementation
  - One ADC with 10-bit resolution
  - Eight analog inputs
    - ADC0 … ADC7
  - 15 kSPS sampling rate
  - 0 – $V_{CC}$ ACD input voltage
  - Selectable reference voltages
    - $AV_{CC}$, 1.1 V, 2.56 V, AREF (external reference)

# ADC (3)

- Conversion Result
  - 10-bit Resolution, Unsigned Mode
    - $ADC = 1024 \cdot \frac{V_{in}}{V_{ref}}$
    - Range: 0 … 1023

# ADC (2)

- Register Mapping



# ADC (4)

- Register Description
  - ADC: ADC Data Register (high and low byte)
  - ADMUX: ADC Multiplexer Selection Register
    - Bit 7:6 – REFS: Reference Selection
    - Bit 4:0 – MUX: Analog Channel Selection
  - ADCSRA: ADC Control and Status Register A
    - Bit 7 – ADEN: ADC Enable
    - Bit 6 – ADSC: Start Conversion

# ADC (5)

- Register Description (continued)
  - ADCSRA (continued)
    - Bit 5 – ADATE: Auto Trigger Enable
      - `Depends on ADTS[2:0] in ADCSRB`
      - `Usually 0: free running mode`
    - Bit 4 – ADIF: ADC Interrupt Flag
      - Conversion complete indicator
    - Bit 2:0 – ADPS: Prescaler Select

# ADC (6)

- Configuration Example
  - ADC7, $V_{ref}$ = 2.56 V, Prescaler = 64
  - Configure ADC
    - `// Vref = 2.56 V, MUX = ADC7`
      `ADMUX = (3 << REFS0) | (PINA7<< MUX0);`
    - `// Enable ADC, Prescaler = 64`
      `ADCSRA = (1 << ADEN) | (6 << ADPS0);`

# ADC (7)

- Configuration Example (continued)
  - Start conversion
    - `ADCSRA |= (1<<ADSC);`
  - Read result
    - `while (ADCSRA & (1<<ADSC));`
    - `result = ADC;`

# ADC (8)

- Register Summary

| Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|
| **ADCL*** | **ADC7** | **ADC6** | **ADC5** | **ADC4** | **ADC3** | **ADC2** | **ADC1** | **ADC0** |
| **ADCH*** | - | - | - | - | - | - | **ADC9** | **ADC8** |
| **ADCSRA** | **ADEN** | **ADSC** | ADATE | **ADIF** | ADIE | **ADPS2** | **ADPS1** | **ADPS0** |
| ADCSRB | - | ACME | - | - | - | ADTS2 | ADTS1 | ADTS0 |
| **ADMUX** | **REFS1** | **REFS0** | ADLAR | **MUX4** | **MUX3** | **MUX2** | **MUX1** | **MUX0** |
| DIDR0 | ADC7D | ADC6D | ADC5D | ADC4D | ADC3D | ADC2D | ADC1D | ADC0D |

* If ADLAR=0. For ADLAR=1 see manual.

# ADC (9)

- Interrupt Summary

| Source | Description |
|---|---|
| ADC_vect | ADC Conversion Complete |