Analog-to-Digital Converter

ATmega4809

Networks and Embedded Software

Module 4.2.6

by Wolfgang Neff

ADC (1)

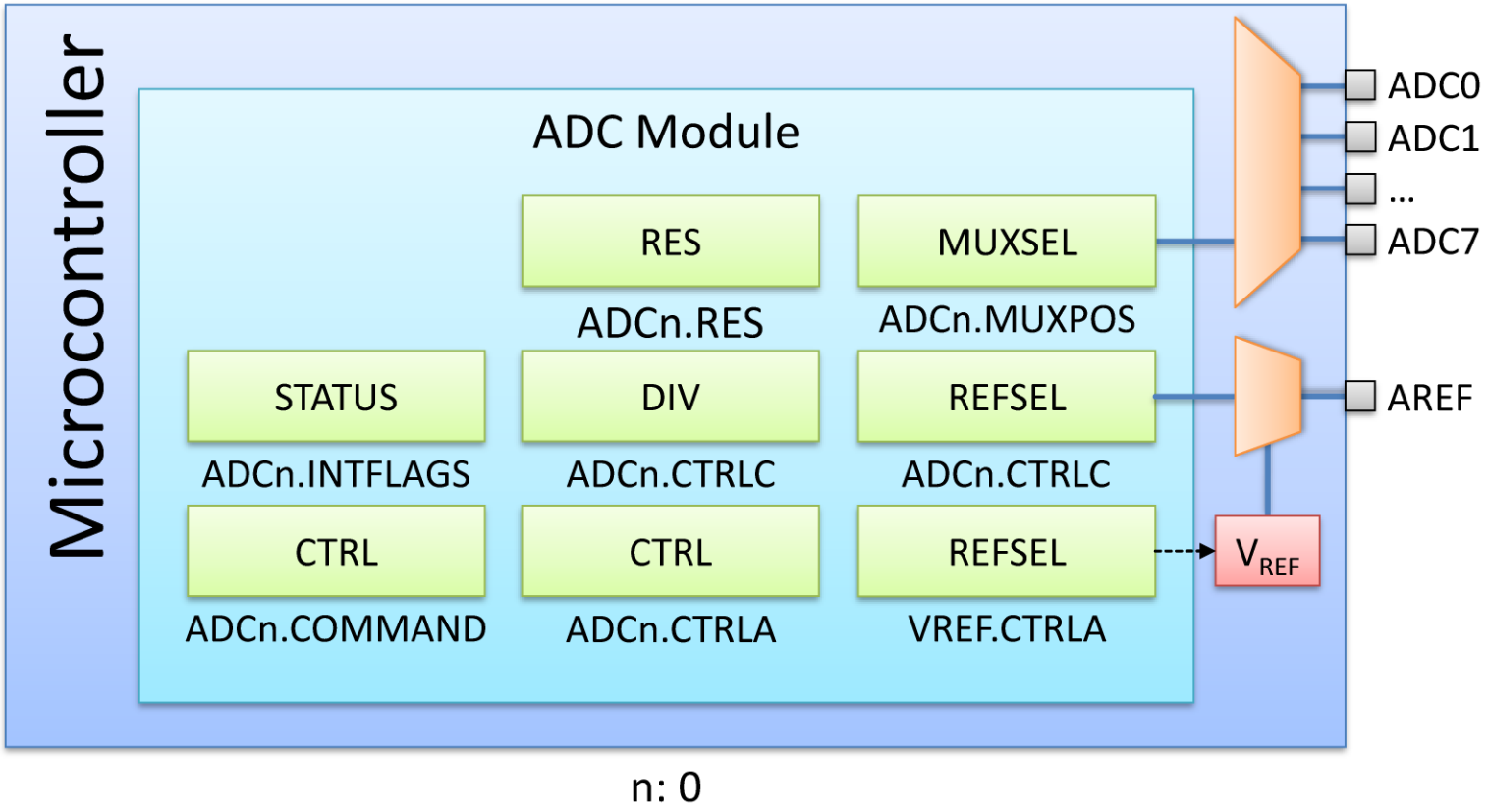
- Implementation
  - One ADC with 10-bit resolution
  - Sixteen analog inputs
    - AIN0 … AIN15
  - 150 kSPS sampling rate
  - 0 – V_{DD} ACD input voltage
  - Selectable reference voltages
    - V_{DD}, 0.55 V, 1.1 V, 1.5 V, 2.5 V, 4.3 V, VREFA (external)

ADC (2)

- Conversion Result
  - 10-bit Resolution, Unsigned Mode
    - $ADC = 1023 \cdot \frac{V_{in}}{V_{ref}}$
    - Range: 0 … 1023

ADC (3)

- Register Mapping



ADC (4)

- Register Description
  - CTRLA: ADC Control Register A
    - Bit 0 – ENABLE: ADC Enable
  - CTRLC: ADC Control Register C
    - Bit 6 – SAMPCAP: Sample Capacitance Selection
      - Set bit if reference voltage is above or equal to 1 V
    - Bit 5:4 - REFSEL: Reference Selection
      - `ADC_REFSEL_INTREF_gc`
      - `ADC_REFSEL_VDDREF_gc`
      - `ADC_REFSEL_VREFA_gc`

ADC (5)

- Register Description (continued)
  - CTRLC: ADC Control Register C (continued)
    - Bits 2:0 – PRESC: Prescaler
      - `ADC_PRESC_DIV2_gc`
      - …
      - Consult datasheet for details
  - MUXPOS: Analog Input Selection Register
    - Bits 4:0 - MUXPOS: Selection on Positive ADC input
      - `ADC_MUXPOS_AIN0_gc`
      - …

ADC (6)

- Register Description (finished)
  - COMMAND: ADC Command Register
    - Bit 0 – STCONV: Start Conversion
  - INTFLAGS: ADC Interrupt Flags Register
    - Bit 0 – RESRDY: Result Ready Interrupt Flag

ADC (7)

- VREF Register Description
  - CTRLA: VREF Control Register A
    - Bit 4:6 – ADC0REFSEL: ADC0 Reference Selection
      - VREF_ADC0REFSEL_0V55_gc
      - VREF_ADC0REFSEL_1V1_gc
      - VREF_ADC0REFSEL_1V5_gc
      - VREF_ADC0REFSEL_2V5_gc
      - VREF_ADC0REFSEL_4V34_gc

ADC (8)

- Configuration Example
  - AIN7, V_{ref} = 1.1 V, Prescaler = 4
  - Configure VREF
    - `VREF.CTRLA = VREF_ADC0REFSEL_1V1_gc;`
  - Configure ADC
    - `ADC.MUXPOS = ADC_MUXPOS_AIN0_gc;`
    - ```
      ADC.CTRLC = ADC_SAMPCAP_bm |
                  ADC_PRESC_DIV4_gc |
                  ADC_REFSEL_INTREF_gc;
      ```
    - `ADC.CTRLA = ADC_ENABLE_bm;`
      ```

ADC (9)

- Configuration Example (continued)
  - Start conversion
    - `ADC.COMMAND = ADC_STCONV_bm;`
  - Read result
    - `while (!(ADC.INTFLAGS & ADC_RESRDY_bm));`
    - `result = ADC.RES;`

ADC (10)

- Register Summary

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTRLA	RUNSTBY	-	-	-	-	RESSEL	FREERUN	**ENABLE**
CTRLB	-	-	-	-	-	SAMPNUM[2:0]		
CTRLC	-	**SAMPCAP**	**REFSEL[1:0]**		-	**PRESC[2:0]**		
CTRLD	IMITDLY[2:0]			ASDV	SAMPDLY[3:0]			
CTRLE	-	-	-	-	-	WINCM[2:0]		
SAMPCTRL					SAMPLEN[4:0]			
MUXPOS					**MUXPOS[4:0]**			

ADC (11)

- Register Summary (continued)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
COMMAND	-	-	-	-	-	-	-	**STCONV**
EVCTRL	-	-	-	-	-	-	-	STARTEI
INTCTRL	-	-	-	-	-	-	WCOMP	RESRDY
INTFLAGS	-	-	-	-	-	-	WCOMP	**RESRDY**
DBGCTRL	-	-	-	-	-	-	-	DBGRUN
TEMP	TEMP[7:0]							

ADC (12)

- Register Summary (finished)

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RES	**RES[7:0]**							
	RES[15:8]							
WINLT	WINLT[7:0]							
	WINLT[15:8]							
WINHT	WINHT[7:0]							
	WINHT[15:8]							
CALIB	-	-	-	-	-	-	-	DUTCYC

ADC (13)

- VREF Register Summary

Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CTRLA	-	**ADC0REFSEL[2:0]**			-	**AC0REFSEL[2:0]**		
CTRLB	-	-	-	-	-	-	ADC0REFEN	AC0REFEN

ADC (14)

- Interrupt Summary

Source	Description
ADCn_RESRDY_vect	Result Ready interrupt
ADCn_WCOMP_vect	Window Comparator interrupt